RT/SYNC	6	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to this pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor adjusted frequency.
EN	7	Enable pin to the regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
VIN1	8	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
PGND1	9	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
SW	10	Regulator switching output. Connect SW to an external power inductor
PGND2	11	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
VIN2	12	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.
BOOT	13	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
NC	14	Not Connection.

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Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT}	Output voltage range	1	36	V
T_J	Operating junction temperature	-40	150	℃

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM)	-2	+2	kV
	Charged Device Model(CDM)	-1	+1	kV

PARAMETER	THERMAL METRIC	QFN-14L	UNIT

R * n /Span <

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V_{IN}=24V, T_A=-40℃~1 25℃, typical value is tested under 25℃.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.5		36	V
I_{SHDN}						

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{PG_OV}	Power-good flag over voltage tripping threshold	POWER BAD (% of FB voltage)		110		%
		POWER GOOD (% of FB voltage)		105		%
I_{PG}	PWRGD leakage current at high level output	VPull-Up = 5V			200	nA
V_{PG_LOW}	PWRGD low level output voltage	IPull-Up = 1 mA		0.05		V
$t_{PGDFLT(rise}$	Delay time to PGOOD high signal			2		ms
$t_{PGDFLT(fall}$	Glitch filter time constant for PGOOD function			100		us
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		110		%
		V_{FB}/V_{REF} falling		105		%
V_{BOOTUV}	BOOT-SW UVLO Threshold	BOOT-SW falling		2.35		V
		Hysteresis		250		mV
T_{SD}	Thermal shutdown threshold*	T_J rising		172		℃
		Hysteresis		12		℃

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Figure 2. Efficiency, F_{SW}=400KHz, V_{OUT}=5V(BIAS)

Figure 3. Efficiency, F_{SW}=400KHz, V_{OUT}=5V(NO BIAS)

Figure 4. Efficiency, F_{SW}=400KHz, V_{OUT}=3.3V

Figure 5. Efficiency, F_{SW}=1.8MHz, Vin=12V

Figure 6. Load Regulation (Vout=5V)

Figure 7.Clock Frequency vs RT/CLK Resistor

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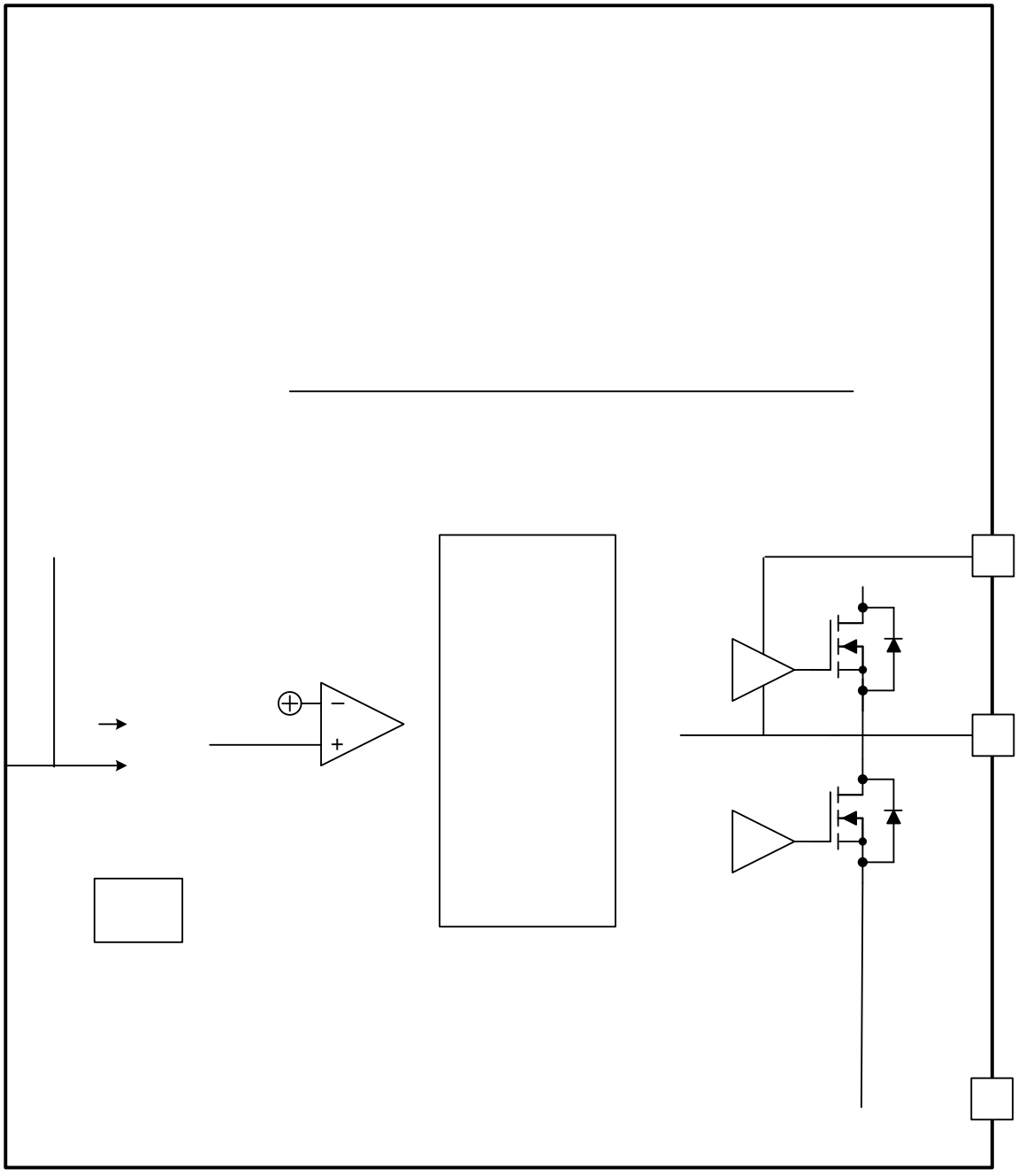

Figure 8. Functional Block Diagram

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Overview

The SCT2464 is a 3.5V-36V input, 6A output, EMI friendly synchronous buck converter with built-in 30m Rdson high-side and 18m Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 200kHz to 1.8MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external component sizes. The SCT2464 features an internal 2ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 13uA (VBIAS=5V) under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the

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Enable and Under Voltage Lockout

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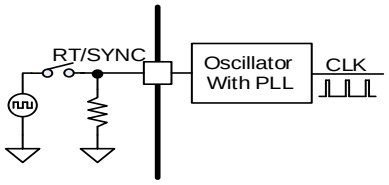

where, fsw is switching clock frequency

Figure 10. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/SYNC pin. The synchronization frequency range is from 200KHz to 1.8MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/SYNC pin with typical 66ns time delay. A square wave clock signal to RT/SYNC pin must have high level no lower than 3V, low level no higher than 0.4V, and pulse width larger than 100ns (TYP).

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 10. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Frequency Spread Spectrum

To reduce EMI, the SCT2464 implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the adjusted switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency adjusted by resistor placed at RT/CLK pin and an external clock synchronization application.

VCC LDO, VCC UVLO, and BIAS Input

The VCC pin is the output of the internal LDO used to supply the control circuits of the SCT2464 and the typical output voltage is 4.2V. The BIAS pin is the input of the internal LDO. This input can be connected to V_{OUT} to save the power loss from V_{IN}. If the BIAS voltage is larger than 4.8V, LDO is powered by BIAS pin. If the BIAS voltage is less than 4.6 V, VIN1 and VIN2 directly powers the internal LDO. To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.6V and hysteresis of 250mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.35V, BOOT UVLO occurs. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output,The duty cycle is large and reaches the minimum-off time(200nS), SCT2464 operates in Low Drop-Out LDO mode.The switching frequency starts to decrease, and the minimum decreases to 80kHZ. To ensure that the output voltage can better follow the change of input voltage.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e.

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Typical Application

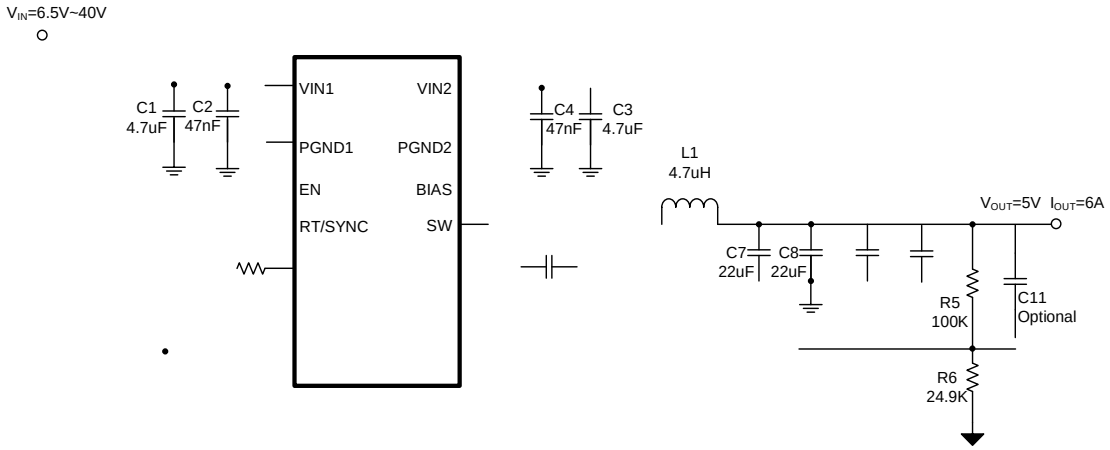

Figure 12. SCT2464 Design Example, 5V Output with Adjustable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 3.5V to 36V
Output Voltage	5V
Maximum Output Current	6A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	6.2mV
Transient Response 1.5A to 4.5A load step	Vout = 300mV
Start Input Voltage (rising VIN)	6.3V
Stop Input Voltage (falling VIN)	5.5V

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Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 24.9K . Use equation 5 to calculate R5.

V_{OUT}

——— (5)

where:

V_{REF} is the feedback reference voltage, typical 1V

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V_{ENR}=1.25V, V_{ENF}=1.05V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 9.

(9)

Where

I_{LPP} is the inductor peak-to-peak current
L is the inductance of inductor
f_{SW} is the switching frequency
V_{OUT} is the output voltage
V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 10 to calculate the inductance value.

(10)

Where

L_{MIN} is the minimum inductance required
f_{sw} is the switching frequency
V_{OUT} is the output voltage
$V_{IN(max)}$ is the maximum input voltage
$I_{OUT(max)}$ is the maximum DC load current
LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the

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the SCT2464 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The s

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(16)

Where

is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
$V_{IN}$is the input voltage

Due to degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 47

Table 3: Typical External Component Values

	57.6					
	57.6					
	274					
	274					

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Application Waveforms

Vin=24V, Vout=5V, unless otherwise noted

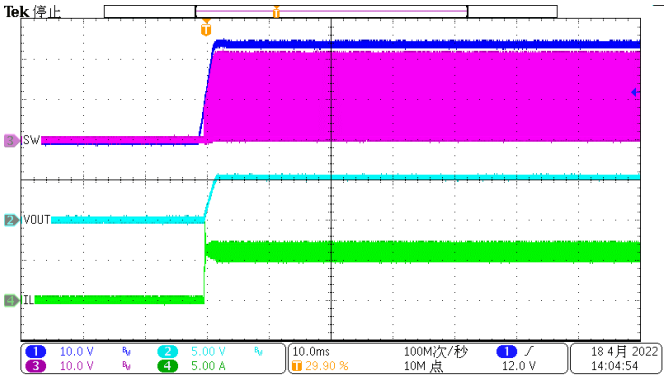

Figure 13. Power up(Iload=6A)

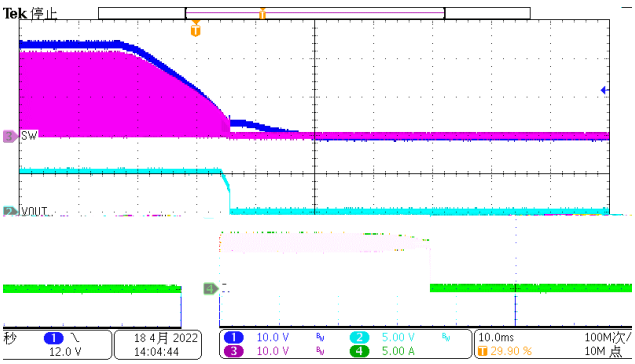

Figure 14. Power down(Iload=6A)

Figure 15. EN toggle (Iload=0.1A)

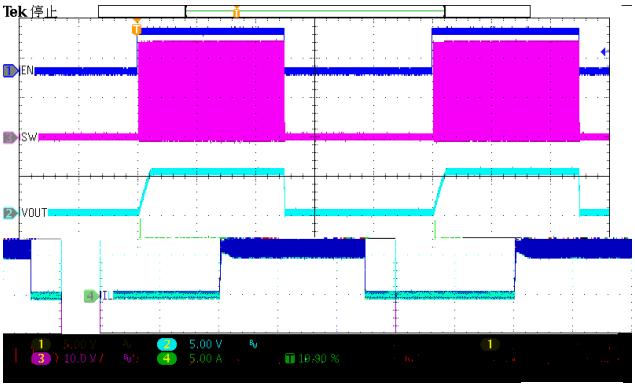

Figure 16. EN toggle (Iload=6A)

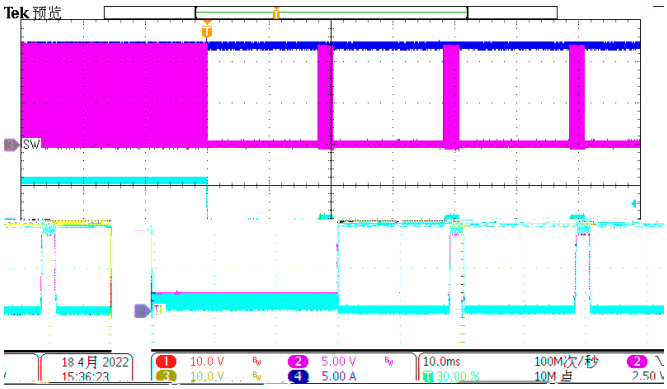

Figure 17. Over Current Protection(1A to hard short)

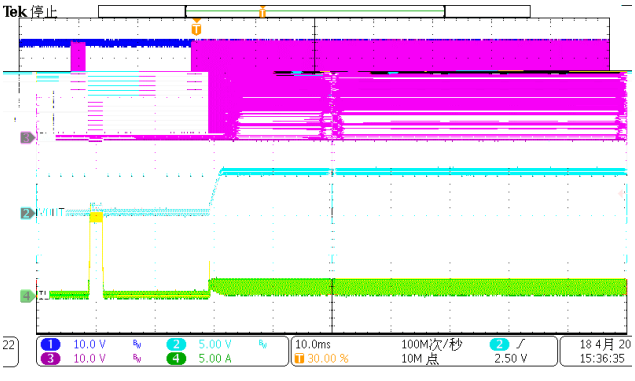

Figure 18. Over Current Release (hard short to 1A)

Application Waveforms

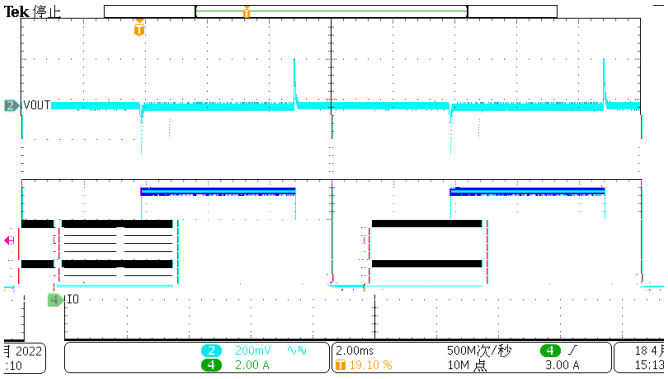

Figure 19. Load Transient (0.6A-5.4A, 1.6A/us)

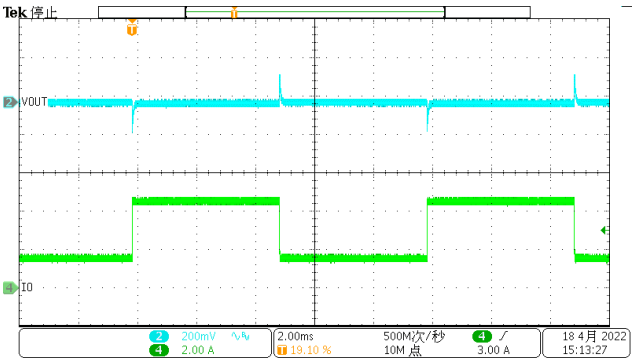

Figure 20. Load Transient (1.5A-4.5A, 1.6A/us)

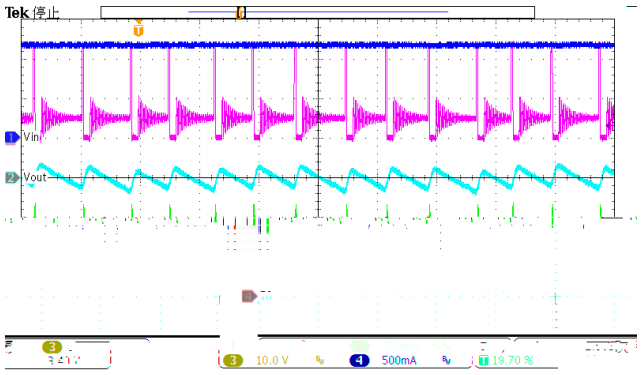

Figure 21. Output Ripple (Iload=100mA)

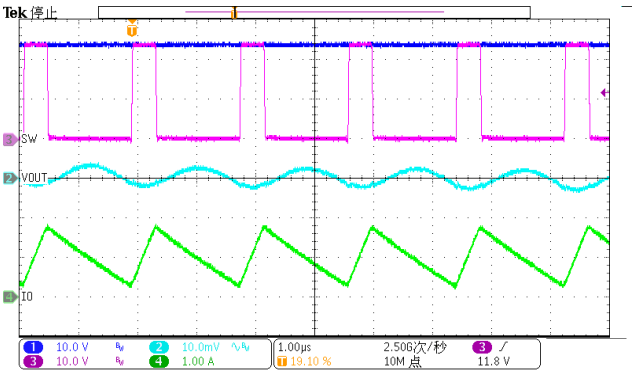

Figure 22. Output Ripple (Iload=1A)

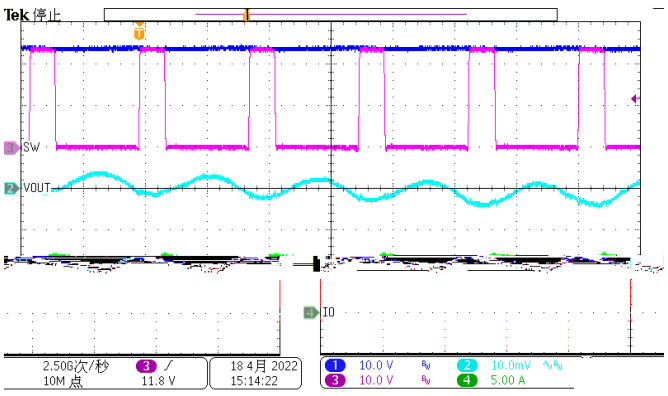

Figure 23. Output Ripple (Iload=6A)

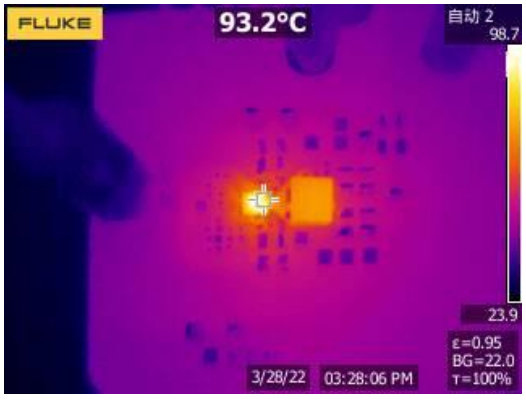

Figure 24. Thermal,12Vin,5Vout,6A

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Layout Guideline

Proper PCB layout is a critical for SCT2464 . The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and PGND as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. The RT/SYNC terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
5. UVLO adjust and RT resistors and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
6. For achieving better thermal performance, a four-layer layout is strongly recommended.

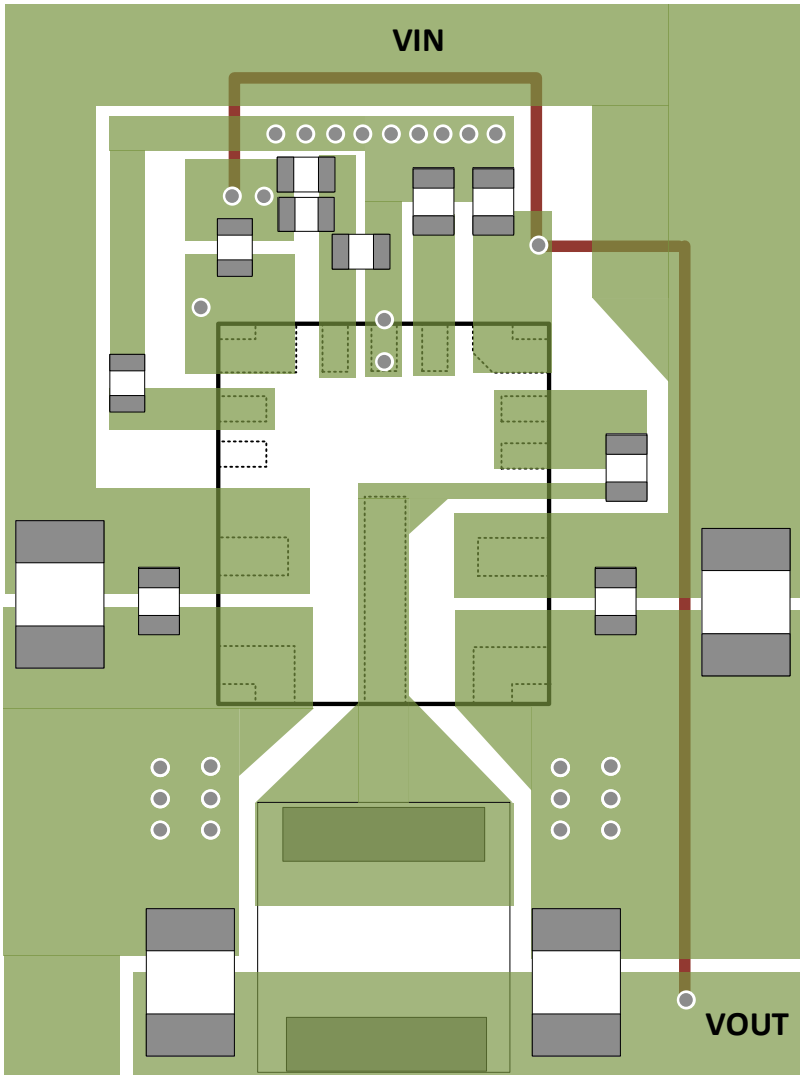

Figure 25. PCB Layout Example

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TOP VIEW

BOTTOM VIEW

SIDE VIEW

SECTION A-A

RECOMMENDED LAND PATTERN

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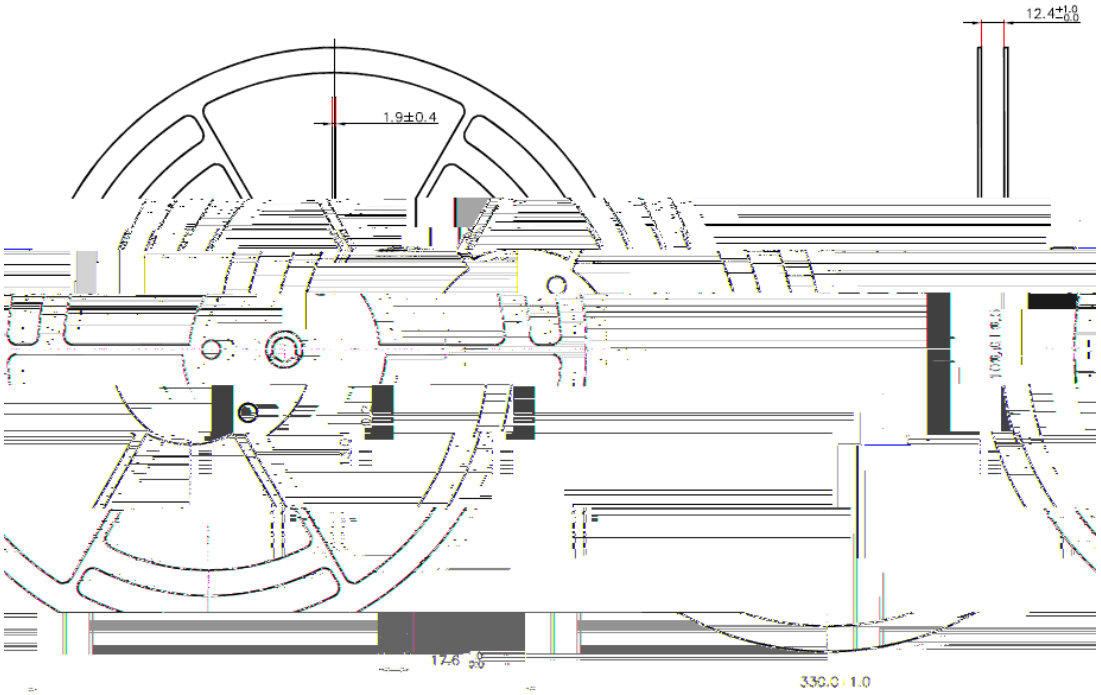
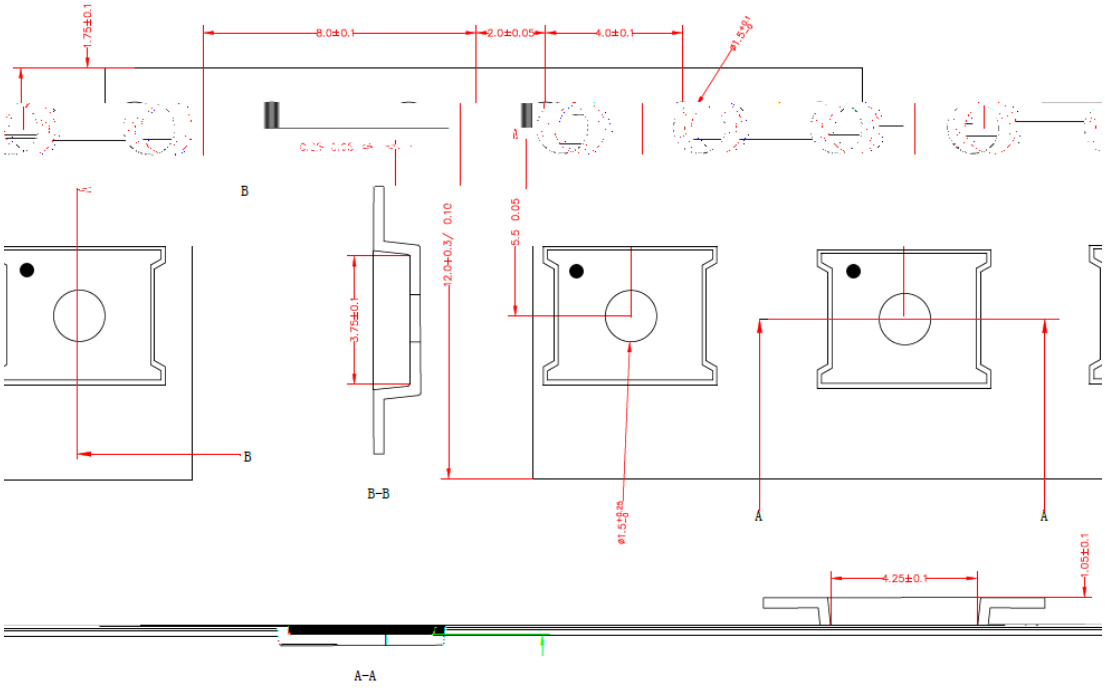

12.4+1.0 0.0
1.9±0.4
17.6 0.0
330.0±1.0


1.75±0.1
8.0±0.1
2.0±0.05
4.0±0.1
ø1.5 0
B
B
3.75±0.1
12.0+0.3/ 0.10
5.5 0.05
B-B
ø1.5 0
A
A
4.25±0.1
1.05±0.1
A-A