17

Wide Input Voltage: 4.2V-17V
4A Continuous Output Current with Integrated 50m /24m FETs
Wide Output Voltage Range:0.8V-7V
Quiescent Current 220uA
Cycle-by-Cycle Current Limiting
Internal 3ms Soft-Start Limits the inrush current
Fixed 800kHz Switching Frequency
Input Under-Voltage Lockout
Power save mode at light load
Over-Temperature Protection
Available in a SOT563 Package

Flat Panel Digital TV and Monitors
Surveillance
Set Top Boxes
Networking Systems
Consumer Electronics
General Purpose

The SCT2240 is a fully integrated high efficiency synchronous step-down DCDC converter capable of delivering 4A current. The devices operate over a wide input voltage range from 4.2V to 17V and fully integrate high-side power MOSFETs and synchronous MOSFETs with very low Rdson to minimize the conduction loss.

With 800 kHz switching frequency, low output voltage ripple, small external inductor and capacitor size are achieved. SCT2240 adopts adaptive constant ON-time control architecture to achieve fast load transient responses for step-down applications.

The SCT2240 operates in power saving mode, which maintains high efficiency during light load operation.

It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2240 requires a minimal number of external components and is available in a space-saving SOT563 package.

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

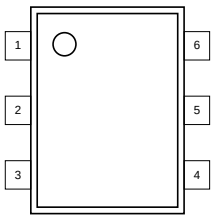
Revision 1.1: Update efficiency curve and Thermography

Revision 1.2: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2240TVAR	Tape & Reel	5000	2240	6	SOT563-6L

Over operating free-air temperature unless otherwise noted(1)

SYMBOL	RATING	UNIT
V_{IN}	-0.3 to 19	V
V_{SW}	-1 to 19	V
V_{SW} <10ns	-2.5 to 21	V
V_{BST}	V_{SW}-0.3 to V_{SW}+6	V
V_{FB}	-0.3 to 6.5	V
V_{EN}	-0.3 to 6.5	V
T_J (2)	-40 to 125	C
T_{STG}	-65 to 150	C



SOT563 Top View

(1.6mm x 1.6mm)

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

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NAME	PIN	PIN FUNCTION
VIN	1	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
SW	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
GND	3	Power ground. Must be soldered directly to ground plane.
BST	4	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
EN	5	Enable logic input. The device has precision enable thresholds 1.215V rising / 1.12V falling for programmable UVLO threshold and hysteresis.
FB	6	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.2	17	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	SOT563	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	120	°C/W
$R_{\theta JB}$	Junction to case thermal resistance(1)	8	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JB}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JB}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2240 are mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2240. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JB}$.

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V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.2		17	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		4.0 350		V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1.2		uA
I_Q	Quiescent current	EN=2V, No load, No switching. VIN=12V. BST-SW=5V		220		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.215		V
V_{EN_L}	Enable low threshold			1.12		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			50		
R_{DSON_L}	Low side FET on-resistance			24		
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage	T_J=25°C, CCM	0.788	0.8	0.812	V
Current Limit						
I_{LIM_LSD}	LSD valley current limit		4.1	5	6.7	A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V		800		kHz
t_{ON_MIN}	Minimum on-time			70		ns
t_{OFF_MIN}	Minimum off-time			220		ns
Soft Start Time						
t_{SS}	Internal soft-start time			3		ms
Protection						
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		155 25		°C

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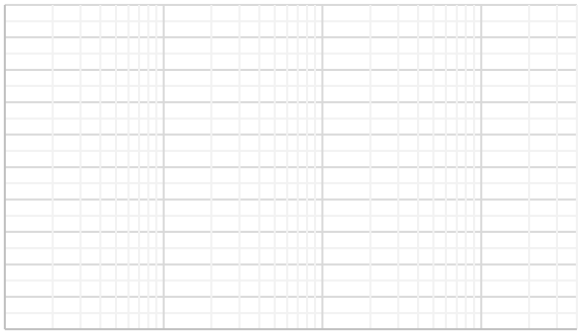

Figure 1. Efficiency vs Load Current(VIN=12V)

Figure 2. Line Regulation

Figure 3. Load Regulation

Figure 4. FB Voltage Vs. Temperature

Figure 5. UVLO Vs. Temperature

Figure 6. Quiescent Current Vs. Temperature

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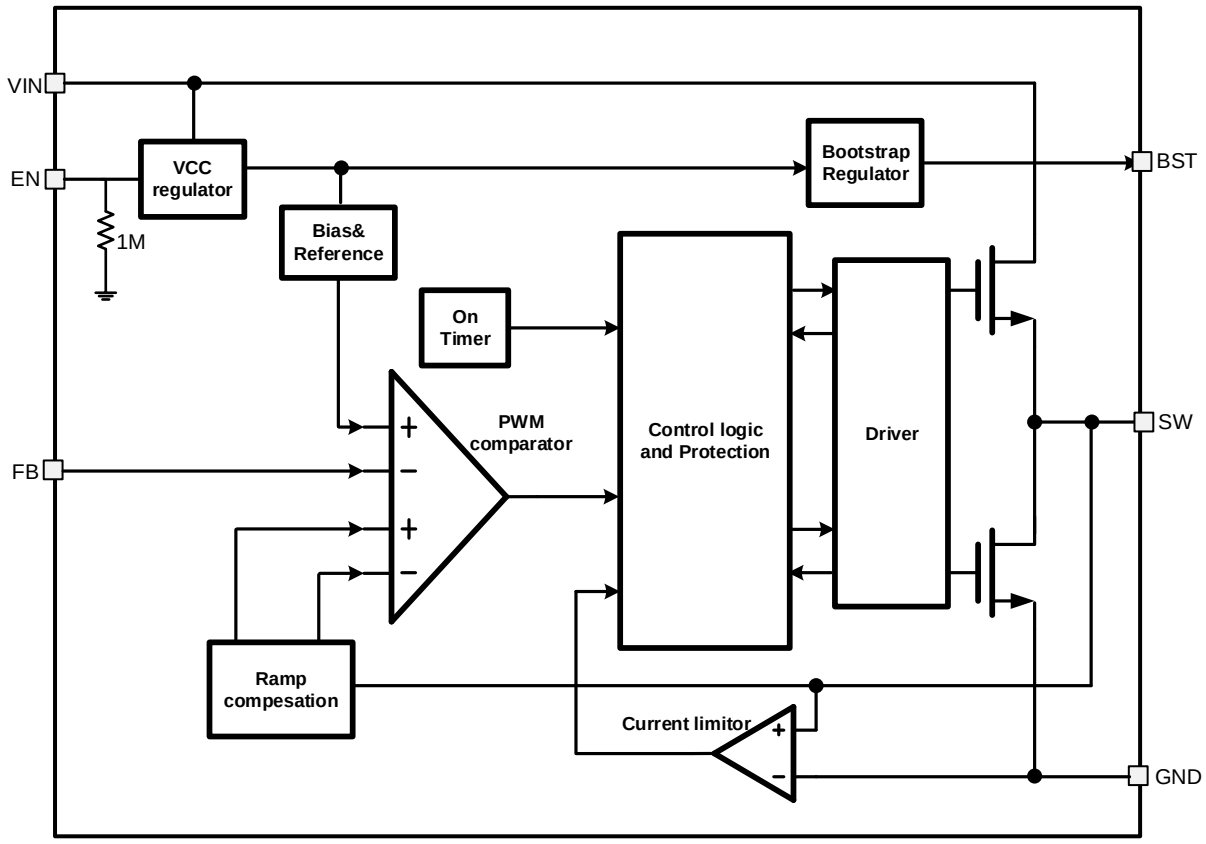

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Adaptive On-time Control

The SCT2240 device is 4.2-17V input, 4A output, synchronous step-down converters with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time - b b Ldc a Lgd b2 d Ld - L 2 L f d 'UHW(c Lgd 2 L L 2 L f d 'UNTS(b b d-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control.

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Under Voltage Lockout UVLO

The SCT2240 Under Voltage Lock Out (UVLO) default startup threshold is typical 4V with VIN rising and shutdown threshold is 3.65V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold

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When the voltage between GND pin and SW pin is lower than the over current threshold voltage, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will drop below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles soft-start period.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Thermal Shutdown

Once the junction temperature in the SCT2240 exceeds 155°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 130°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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Typical Application

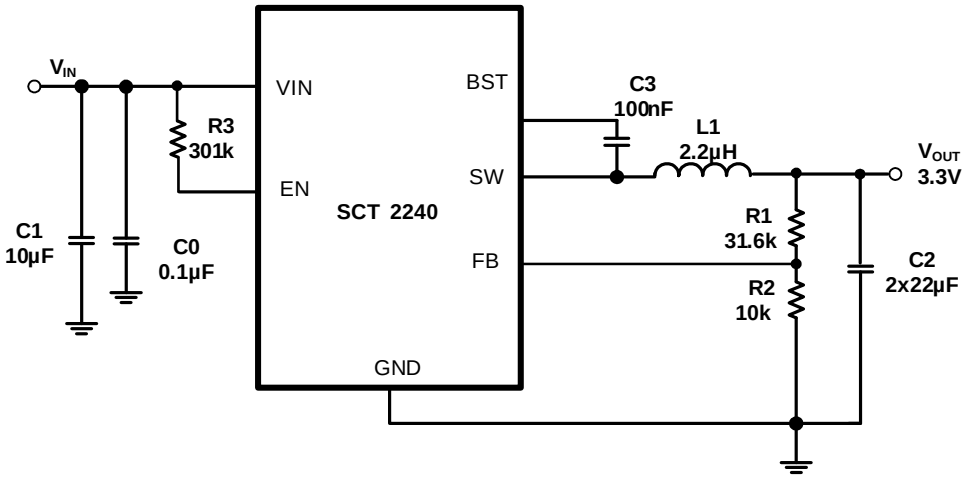

Figure 8. 12V Input, 3.3V/4A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	3.3V
Output Current	4A
Switching Frequency	800kHz

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Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 E - db2 d cdc for the decoupling capacitor and a 0.1 E bd b a - - b b L2 - db2 d cdc to be placed as close as possible to the VIN pin of the SCT2240.

Use Equation (5) to calculate the input voltage ripple:

(5)

$$M \quad \frac{NTS}{M \quad RV} \quad \frac{NT}{M} \quad \frac{NTS}{M}$$

Where:

C_{IN} is the input capacitor value

f_{sw} is the converter switching frequency

I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 25V/10uF input ceramic capacitor is recommended for most of applBT/F3 9.96 Tf1 0 0 1

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$$KOD \quad NTS \quad MC \quad \frac{NTS}{1} \tag{7}$$

Set the current limit of the SCT2240 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The c bL2 - CB d- - L bd 'CBQ(c the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT2240. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744311220 is used on SCT2240 evaluation board.

Table 1. Recommended Inductors

Part Number	L (uH)	DCR Max	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744311220	2.2	11.4	13	7.3x7.2x3.8	Wurth Electronik

Output Feedback Resistor Divider Selection

The SCT2240 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 8. Use equation (8) to calculate the resistor divider values.

$$\frac{NTS \quad e \quad 1}{e} \tag{8}$$

Table 2. Recommended Component Selections

Output Voltage (V)			L (µH)	C1 (µF)	C2 (µF)	C3 (nF)
1.2	4.99	10	1.5	10	2 x 22	100
1.5	8.66	10	1.5	10	2 x 22	100
1.8	12.4	10	2.2	10	2 x 22	100
2.5	21.5	10	2.2	10	2 x 22	100
3.3	31.6	10	2.2	10	2 x 22	100
5.0	52.3	10	3.3	10	2 x 22	100

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Application Waveforms

Vin=12V, Vout=3.3V, unless otherwise noted

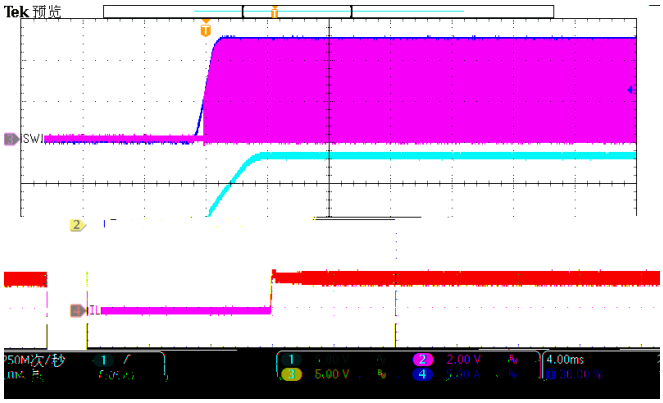

Figure 9. Power up

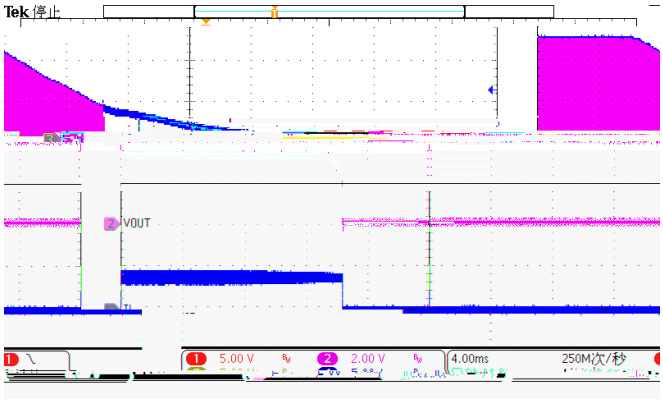

Figure 10. Power down

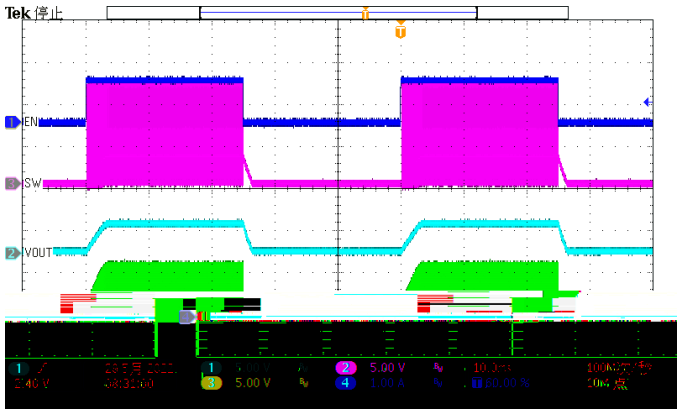

Figure 11. EN toggle Iout=0.1A

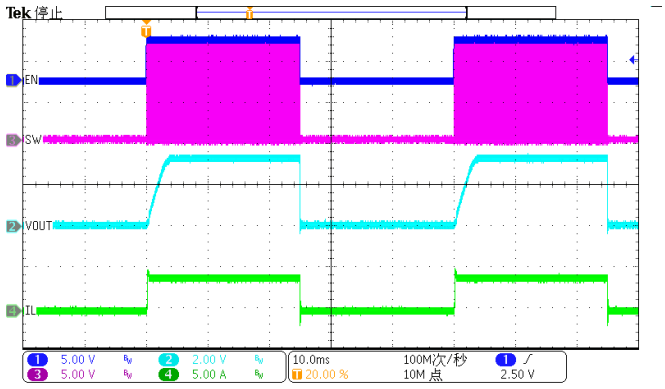

Figure 12. EN toggle Iout=4A

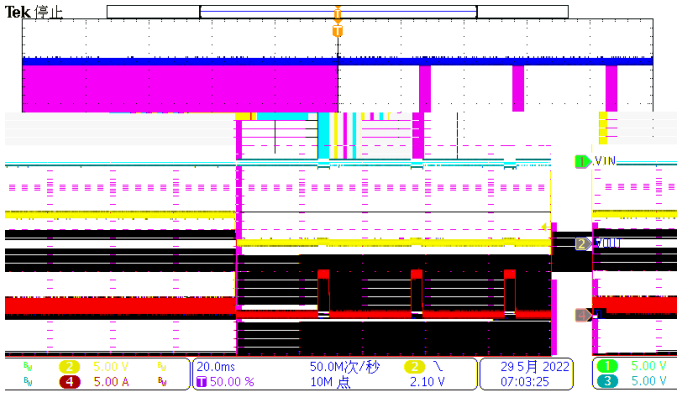

Figure 13. Over Current Protection (1A to hard short)

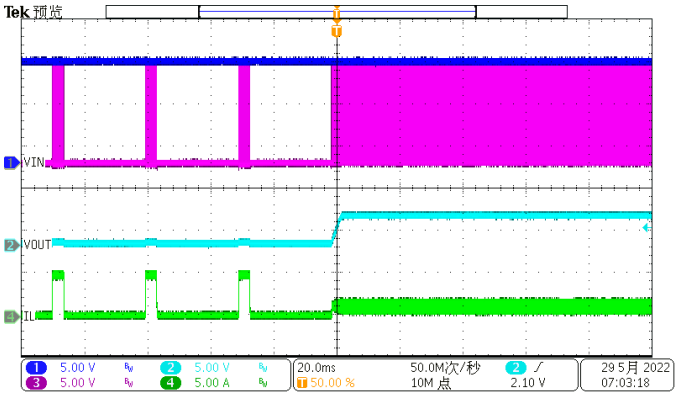

Figure 14. Over Current Release (1A to hard short)

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Application Waveforms

Vin=12V, Vout=5V, unless otherwise noted

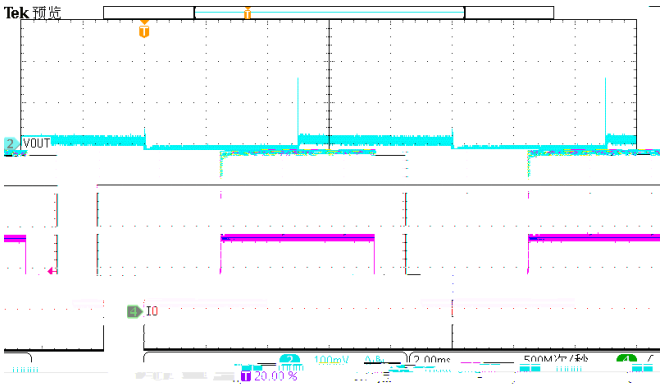

Figure 15. Load Transient (0.4A-3.6A, 1.6A/us)

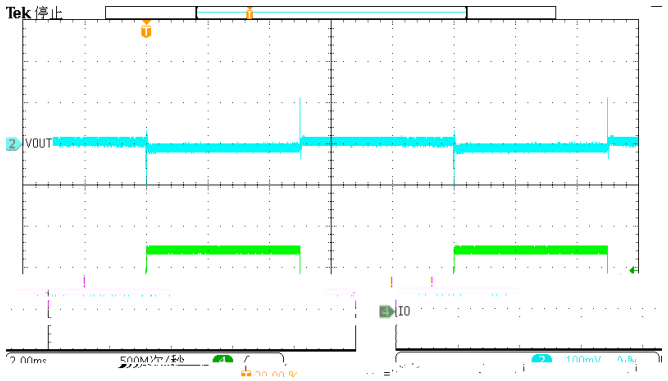

Figure 16. Load Transient (1A-3A, 1.6A/us)

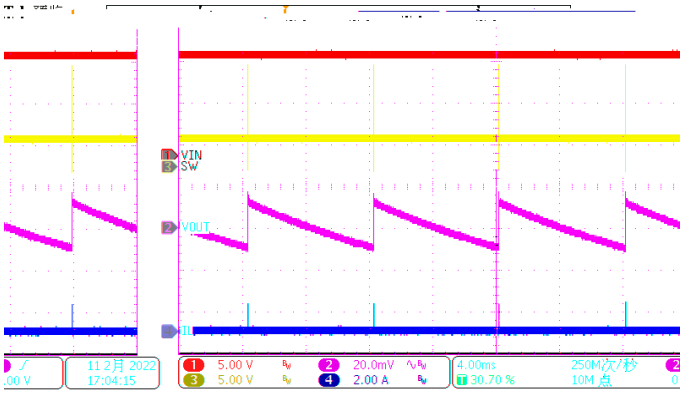

Figure 17. Output Ripple (Iload=0A)

Figure 18. Output Ripple (Iload=0.1A)

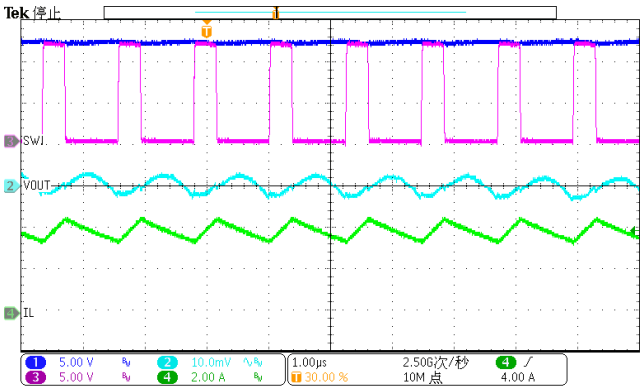

Figure 19. Output Ripple (Iload=4A)

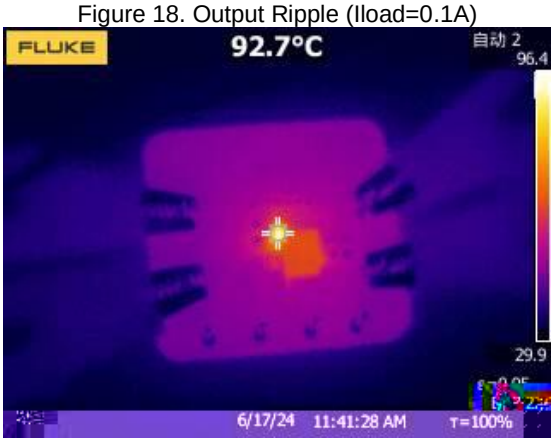

Figure 20. Thermal, 12VIN, 3.3Vout, 4A

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Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 21 is the recommended PCB layout of SCT2240.

The layout needs be done with well consideration of the thermal. A large top layer

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Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (9).

$$C\ L\ W \quad \frac{1}{\mathrm{I}} \tag{9}$$

where

T_A is the maximum ambient temperature for the application.

R_{JA} is the junction-to-ambient thermal resistance.

The real junction-to-ambient thermal resistance R_{JA} of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

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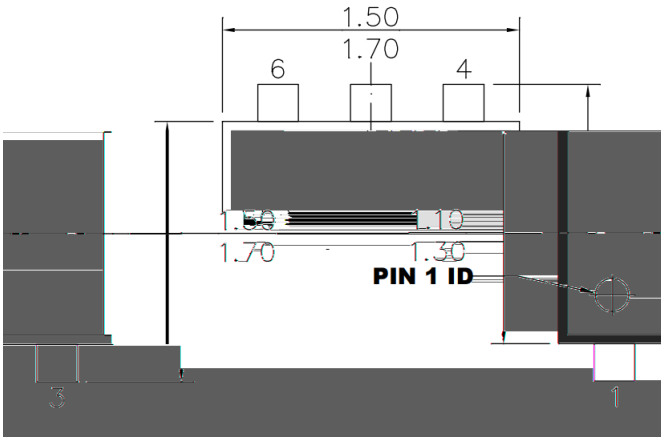
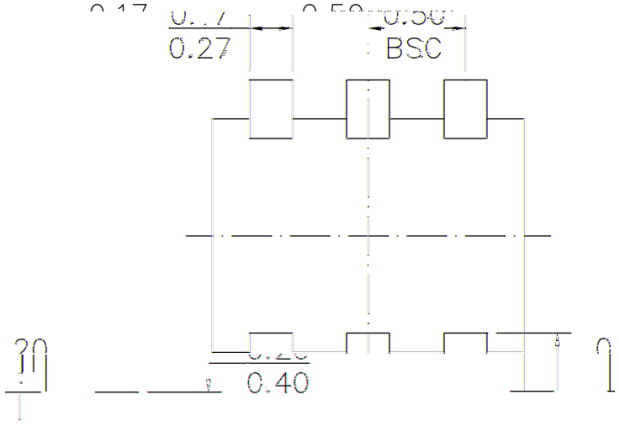
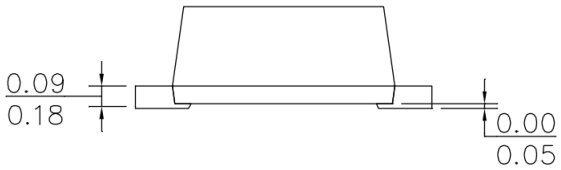


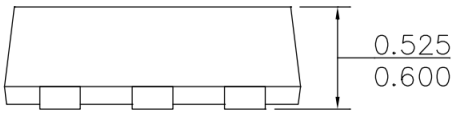
TOP VIEW



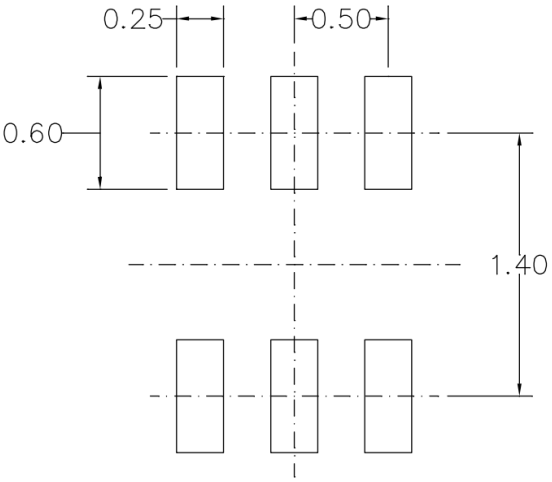
BOTTOM VIEW



SIDE VIEW



FRONT VIEW



RECOMMENDED LAND PATTERN

SOT563-6L Package Outline Dimensions

NOTE:

1. THE LEAD SIDE IS WETTABLE.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4. JEDEC REFERENCE IS MO-220.
5. DRAWING IS NOT TO SCALE.

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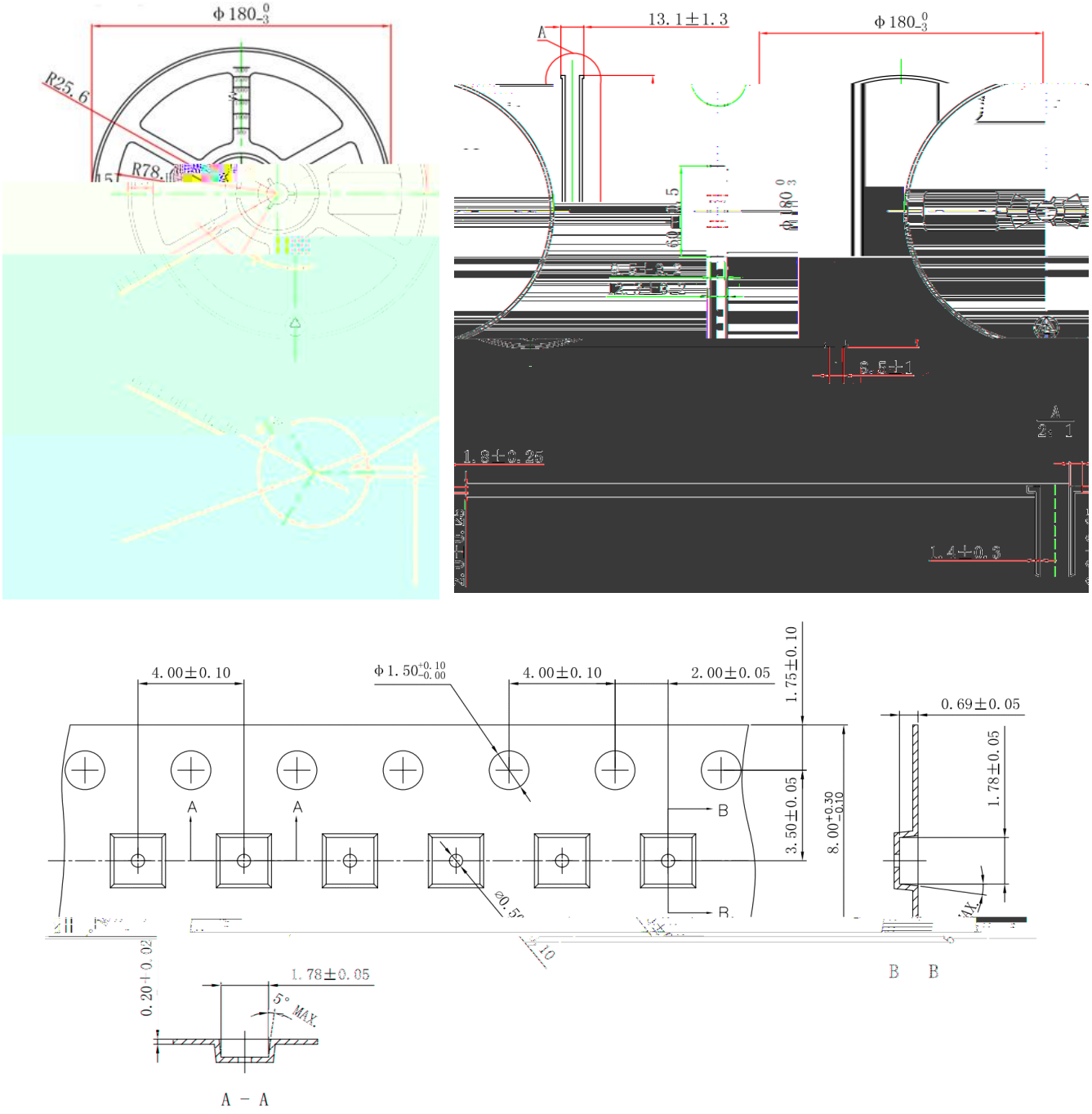

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