

# DrDEDL DJ girgDrg srs Di hs rDHGHGD6Gsri i

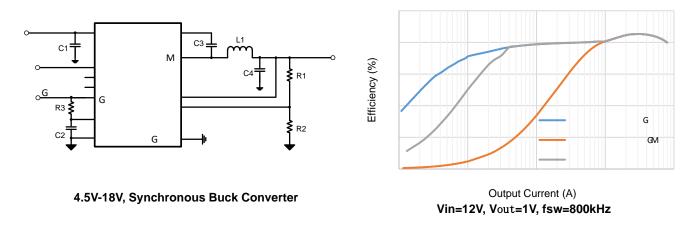
**I EXYVI** 

HI GVMTXMS RD

ETTPMGEXMS R D



### X TNGE PIE TTPMGE XMS RD





#### VI MNS RDL MXS V DD

#### HI MGI IS VHI VIMR S V EXNS RID

ORDERABLE	PACKAGING	STANDARD	PACKAGE	PINS	PACKAGE
DEVICE	TYPE	PACK QTY	MARKING		DESCRIPTION

# EF SPYXIDE MY DVEXNRK D

MIN	MAX	UNIT
	MIN	MIN MAX

#### TNRIGS R NKYVEXNS RD

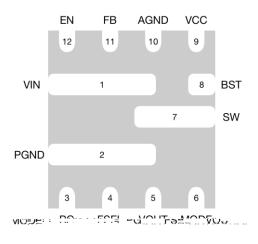


Figure 1. 12-Lead Plastic QFN

(1)

(2)

#### TNRD YRGXNS R D

NAME	NO.	PIN FUNCTION



1	1



## I PI GXVMGE PIGL E VE GXI VMXMG D

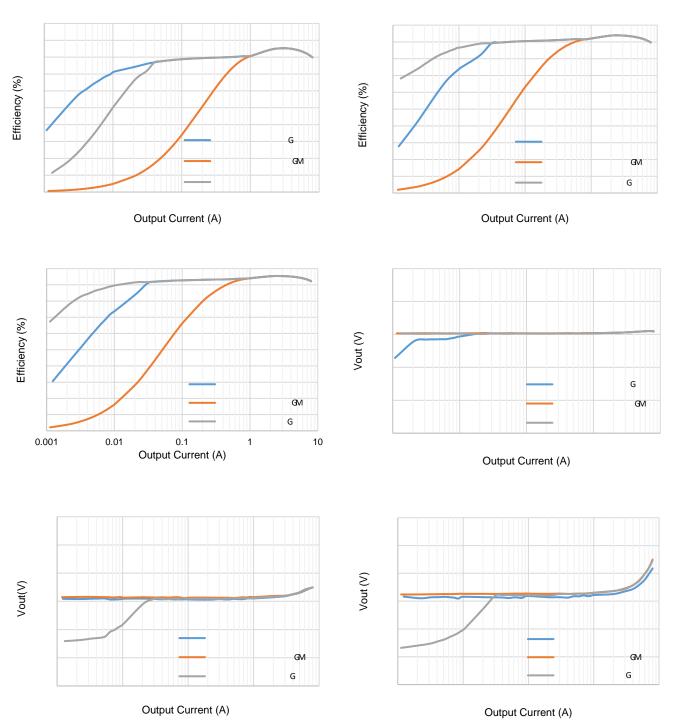
SYMBOL	PARAMETER	TEST CONDITION	MIN	ТҮР	MAX	UNIT
Power Sup	oly and Output					



	SYMBOL P	PARAMETER	TEST CONDITION	MIN	ТҮР	MAX	UNIT
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### X TNGE PIGLE VE GXI VM XNG D



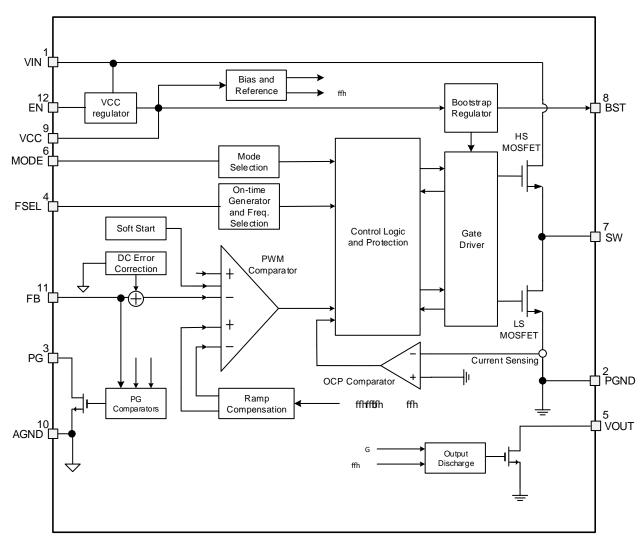
D

D



#### YRGXMS RE PIF PS GOIDHNE KVE D

D



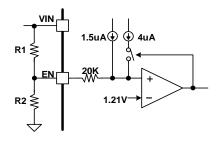
## S TI VEXMS RD

Overview



Enable and Under Voltage Lockout Threshold

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**Output Voltage** 

Internal Soft-Start

**Switching Frequency Selection** 



#### Table 1. FSEL Pin Set-up for Switching Frequency Selection

**Mode Selection** 



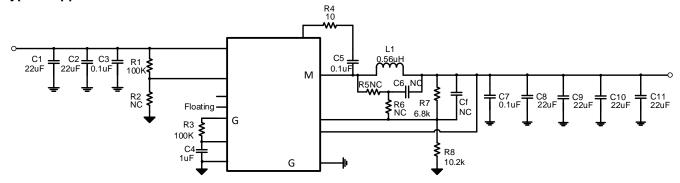
**Over voltage Protection** 

**Thermal Shutdown** 



# ETTPNGEXNS RIMR SV EXNS RD

#### **Typical Application**



Design Parameters				
Design Parameters	Example Value			



Input Capacitor Selection

**Inductor Selection** 

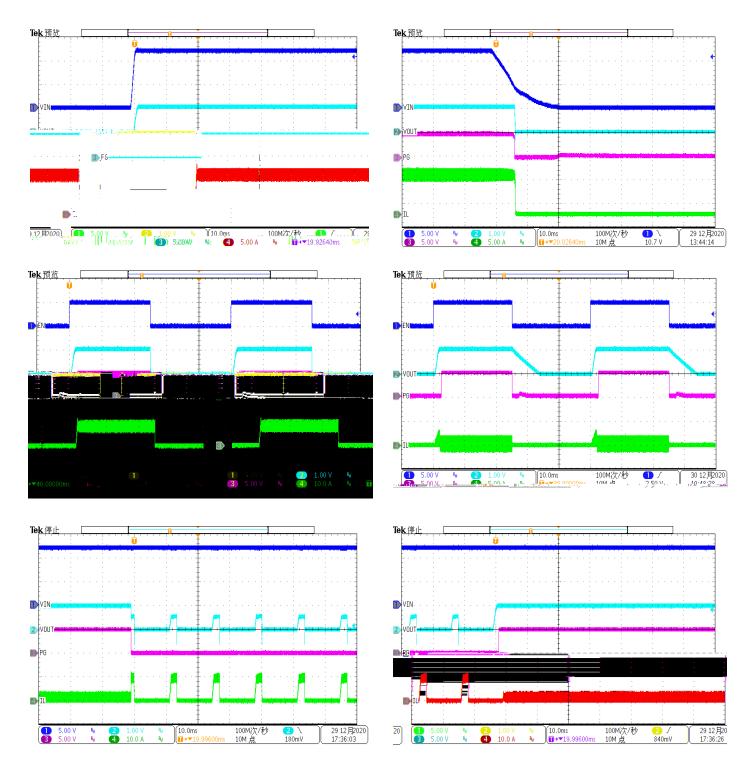


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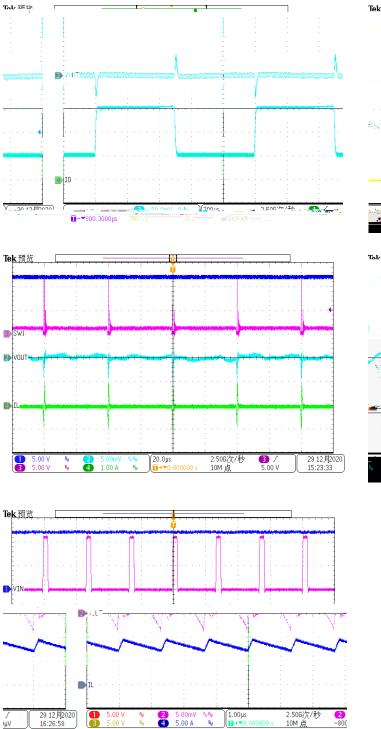
**Output Capacitor Selection** 

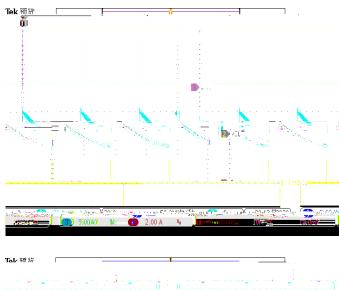


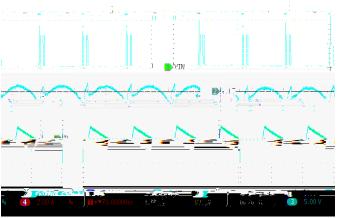
#### **Application Waveforms**

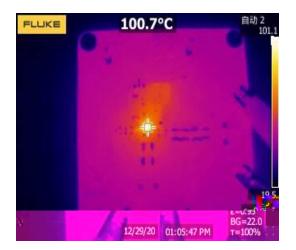


#### Application Waveforms(Continued)









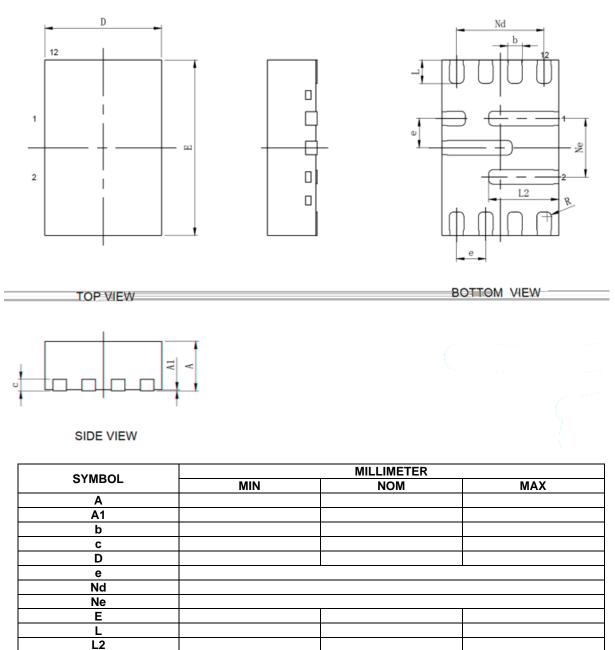


### Layout Guideline

- 1.
- 2.
- **L**.
- 3.
- 4.



### TE GOE KI DAR SV EXNSR



#### NOTE:

1.

2. 3.

3. 4.

4. 5.

D.

D

R



### XETIDERHOVIIPONR SV EXMSRD

SYMPOL	MILLIMETER				
SYMBOL	MIN	NOM	MAX		
A					
B					
С					
D					
t					

SYMBOL	MILLIMETER				
SYMBOL	MIN	NOM	MAX		
E					
F					
P2					
D					
D1					
P0					
W					
Р					
A0					
B0					
К0					
t					

