

V_{in}, 3A Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Voltage: 4.2-17V
- 3A Continuous Output Current with Integrated 70m /42m FETs
- Wide Output Voltage Range:0.8V-7V
- Quiescent Current 275uA
- Cycle-by-Cycle Current Limiting
- Internal 2ms Soft-Start Limits the Inrush Current
- Fixed 750kHz Switching Frequency
- Input Under-Voltage Lockout
- Forced PWM Mode at Light Load
- Over-Temperature Protection
- Available in a SOT563 and TSOT23 Package

APPLICATIONS

- Flat Panel Digital TV and Monitors
- Surveillance
- Set Top Boxes
- Networking Systems
- Consumer Electronics
- General Purpose

DESCRIPTION

The SCT2231 is a fully integrated high efficiency synchronous step-down DCDC converter capable of delivering 3A current. The devices operate over a wide input voltage range from 4.2V to 17V and fully integrate high-side power MOSFETs and synchronous MOSFETs with very low R_{ds(on)} to minimize the conduction loss.

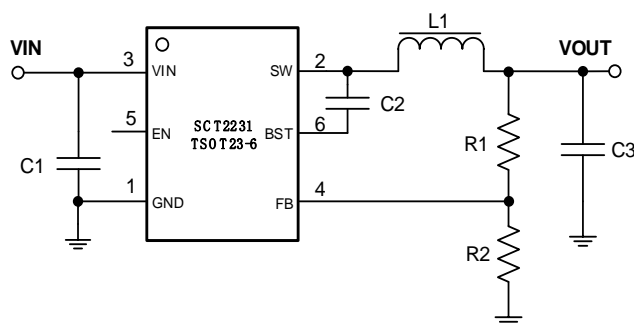
With 750 kHz switching frequency, low output voltage ripple, small external inductor and capacitor size are achieved. SCT2231 adopts adaptive constant ON-time control architecture to achieve fast load transient responses for step-down applications.

The SCT2231 operates in Forced Pulse Width Modulation (FPWM) mode, which maintains small output voltage ripple during light load operation.

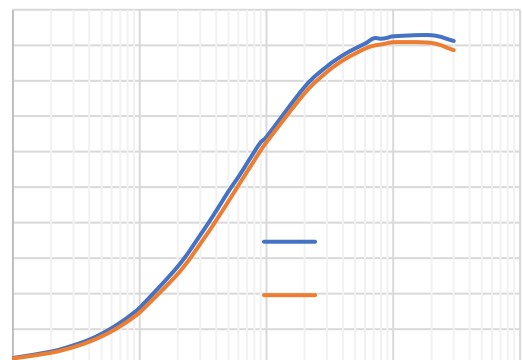
It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2231 requires a minimal number of external components and is available in a space-saving SOT563 and TSOT23-6 package.

TYPICAL APPLICATION



Power Efficiency



SCT2231

REVISION HISTORY

NOTE: Page

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ELECTRICAL CHARACTERISTICS

$V_{IN}=12V$, $T_J=-40^{\circ}C-125^{\circ}C$, typical values are tested under $25^{\circ}C$.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.2		17	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		4.0 300	4.15	V mV

I_{SDQ EMC} /Span

TYPICAL CHARACTERISTICS

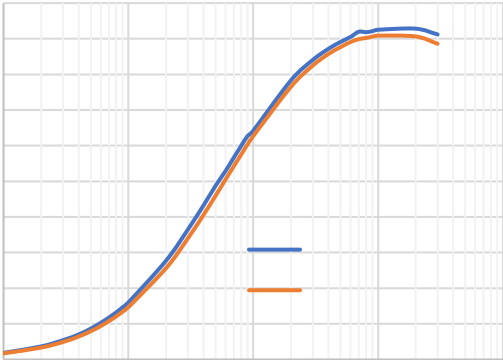


Figure 1. SCT2231 Efficiency, Vin=12V

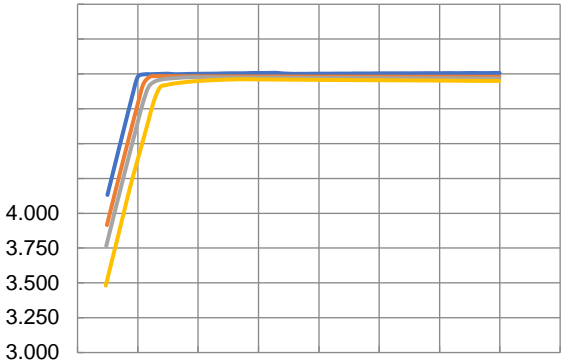


Figure 2. Vout Vs. VIN

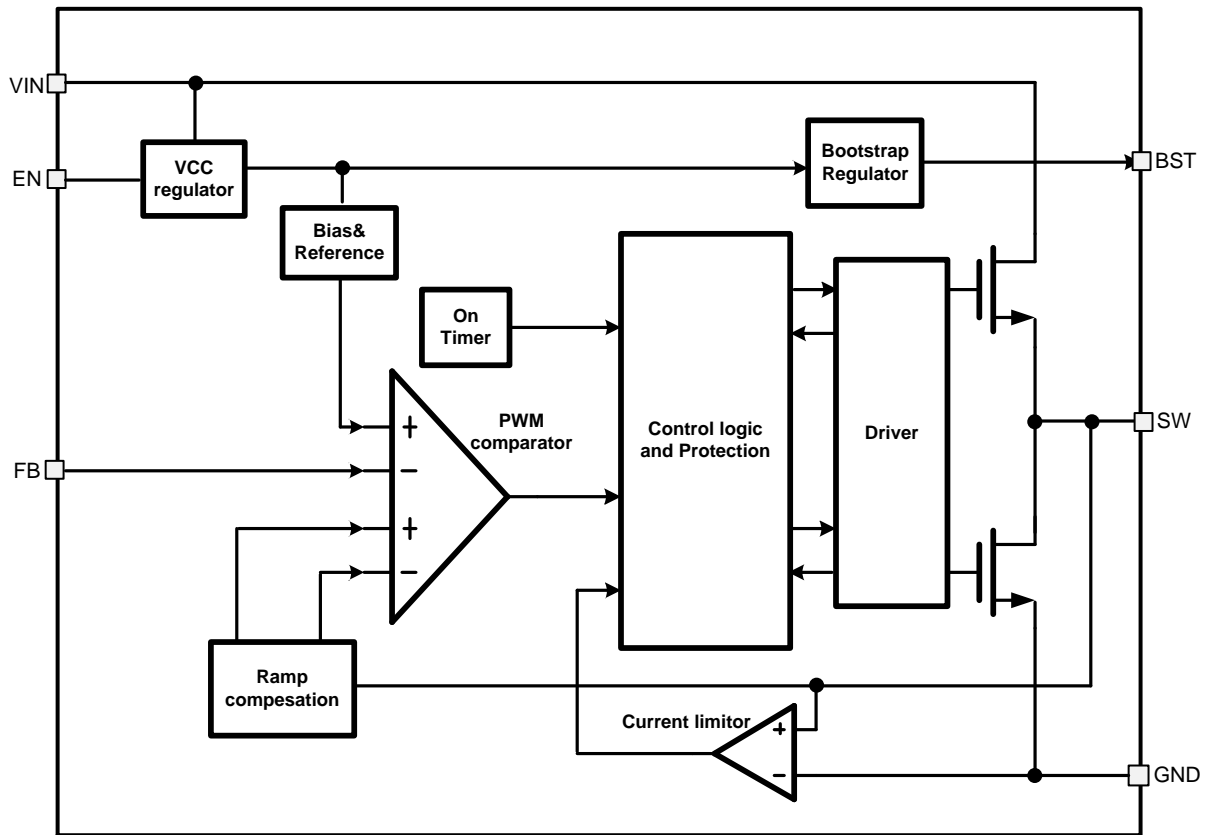
Figure 3. Load Regulation

Figure 4. FB Vs. Temperature

Figure 5. UVLO Vs. Temperature

Figure 6. Line Regulation

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Adaptive On-time Control

The SCT2231 device is 4.2-17V input, 3A output, and synchronous step-down converters with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time

by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT2231 turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2231 turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \cdot f_s} \quad (1)$$

Where:

- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.
- f_s

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An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 5.3uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 7. The resistor divider R3 and R4 are calculated by equation (2) and (3).

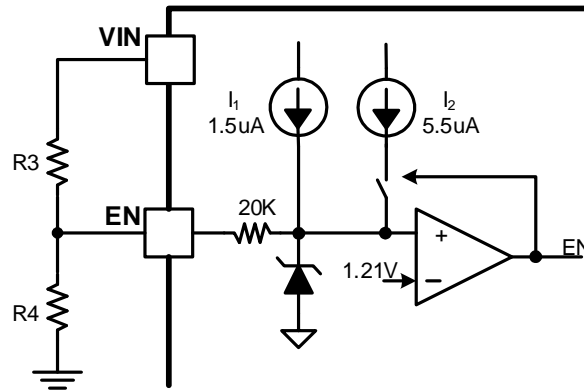


Figure 7. Adjustable VIN UVLO

$$3 = \frac{(I_1 - I_2) R_3}{I_1 R_4 + I_2 R_3} \quad (2)$$

$$4 = \frac{V_{ENR}}{V_{EMF} + V_{ENR} \left(\frac{R_3}{R_4} + 1 \right)} \quad (3)$$

Where:

- Vstart: Vin rise threshold to enable the device
- Vstop: Vin fall threshold to disable the device
- I₁=1.5uA
- I₂=5.5uA
- V_{ENR}=1.18V
- V_{EMF}=1.1V

Thermal Shutdown

Once the junction temperature in the SCT2231 exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

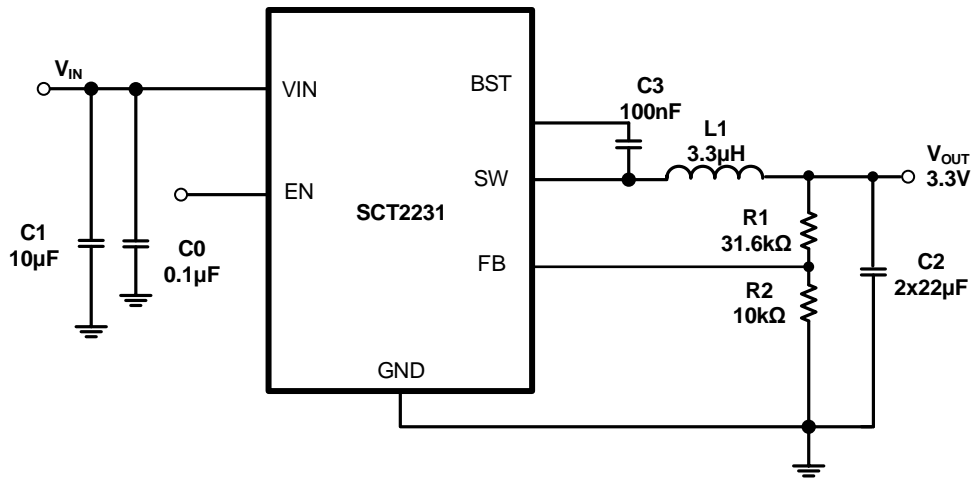


Figure 8. 12V Input, 3.3V/3A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	3.3V
Output Current	3A
Switching Frequency	750kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 for the decoupling capacitor and a 0.1 to be placed as close as possible to the VIN pin of the SCT2231.

Use Equation (4) to calculate the input voltage ripple:

$$= \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{1}{x}) \quad (4)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage

ripple less than 100mV. Generally, a 25V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of inductor affects the power behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maximum load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (5).

$$L = \frac{V_{in} \times (V_{in} - V_{out})}{\Delta I \times f_{sw} \times \eta} \tag{5}$$

Where:

K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK} , is calculated as in equation (6).

$$I_{LPEAK} = I_{OUT} + \Delta I \tag{6}$$

Set the current limit of the SCT2231 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT2231. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744325330 is used on SCT2231 evaluation board.

Table 1. Recommended Inductors

Part Number	L (uH)	DCR Max (mΩ)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744325330	3.3	5.9	15	10.5x10.5x4.7	Würth Elektronik

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Output Feedback Resistor Divider Selection

The SCT2231 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 8. Use equation (7) to calculate the resistor divider values.

$$V_1 = \frac{(V_{in} - V_{out}) \times R_2}{R_1 + R_2} \quad (7)$$

Table 2. Recommended Component Selections

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C1 (μF)	C2 (μF)	C3 (nF)
1.2	4.99	10	1.5	10	2 x 22	100
1.5	8.66	10	1.5	10	2 x 22	100
1.8	12.4	10	2.2	10	2 x 22	100
2.5	21.5	10	2.2	10	2 x 22	100
3.3	31.6	10	3.3	10	2 x 22	100
5.0	52.3	10	3.3	10	2 x 22	100

Application Waveforms

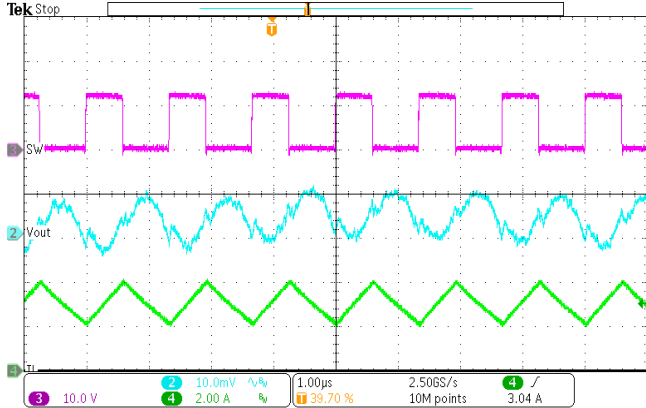


Figure 9. SW node waveform and Output Ripple
VIN=12V, IOUT=3A

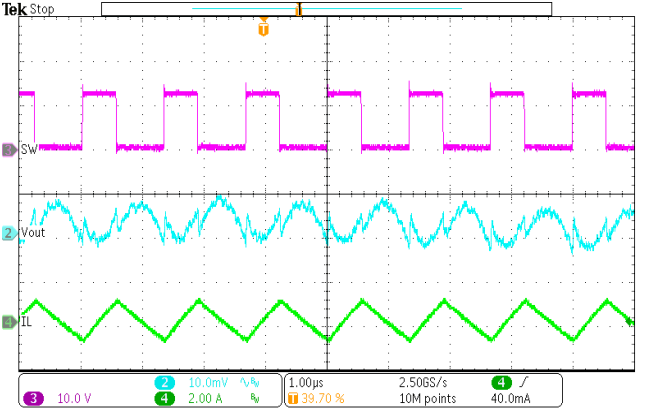


Figure 10. SW node Waveform and Output Ripple
VIN=12V, IOUT=10mA

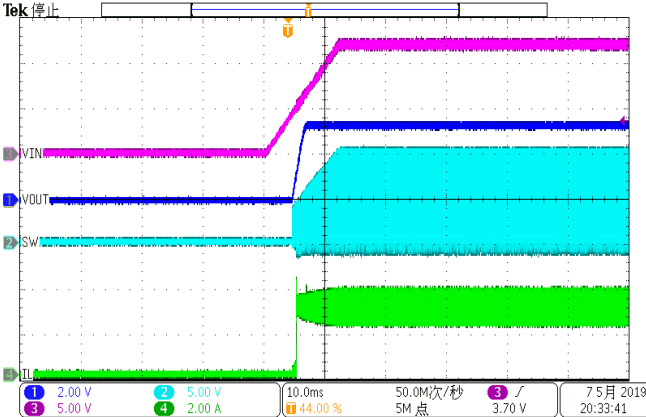


Figure 11. Power Up
VIN=12V, VOUT=3.3V, IOUT=3A

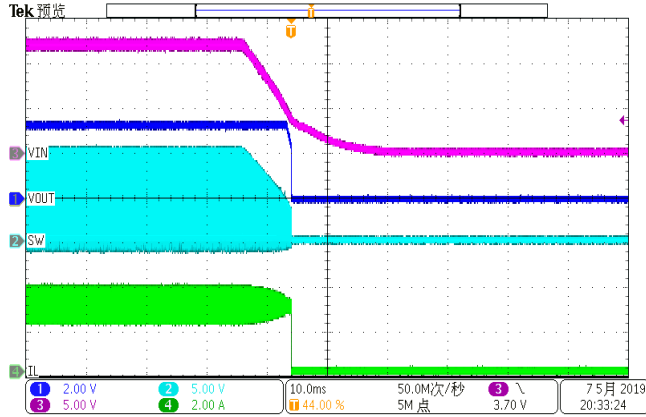


Figure 12. Power Down
VIN=12V, VOUT=3.3V, IOUT=3A

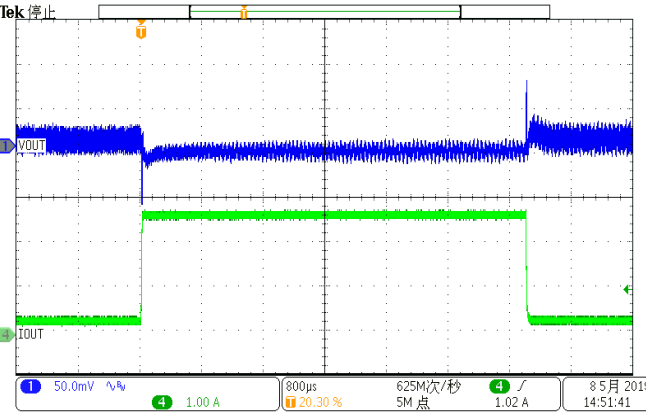


Figure 13. Load Transient
VOUT=3.3V, IOUT=0.3A to 2.7A, SR=250mA/us

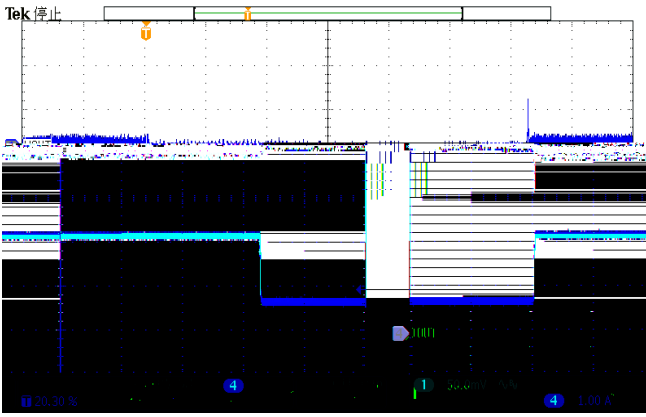


Figure 14. Load Transient
VOUT=3.3V, IOUT=0.75A to 2.25A, SR=250mA/us

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 15 is the recommended PCB layout of SCT2231.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

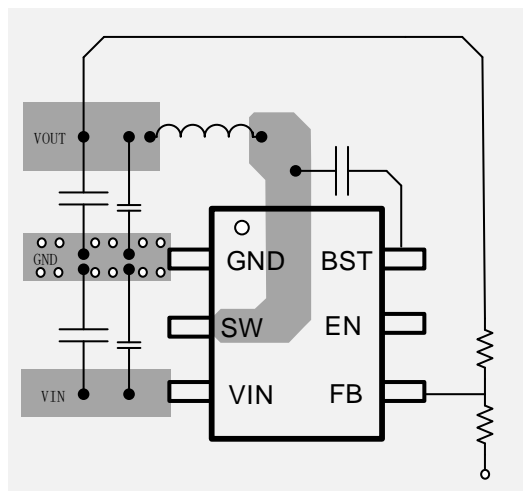


Figure 15. PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (8).

$$T_J = \frac{125 - T_A}{R_{JA}} \quad (8)$$

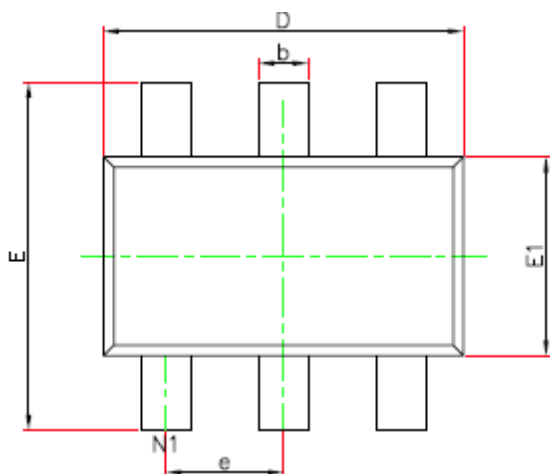
where

T_A is the maximum ambient temperature for the application.

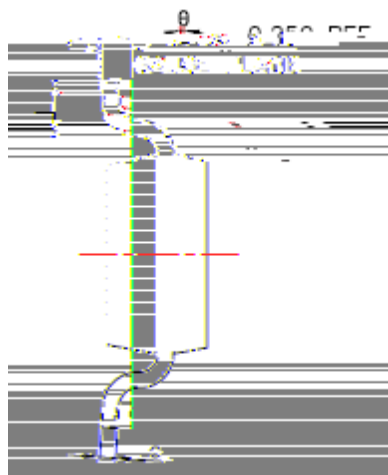
R_{JA} is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance R_{JA} of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

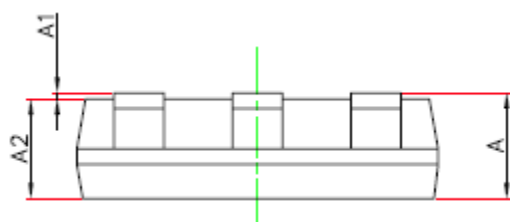
PACKAGE INFORMATION (TSOT23-6)



TSOT23-6 TOP VIEW



TSOT23-6 BOTTOM VIEW



TSOT23-6 SIDE VIEW

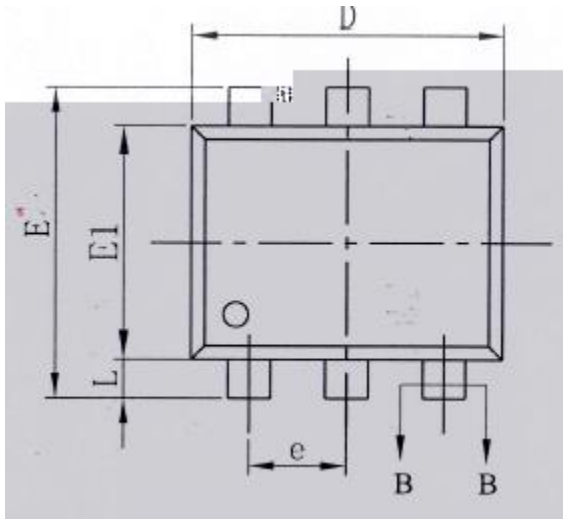
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

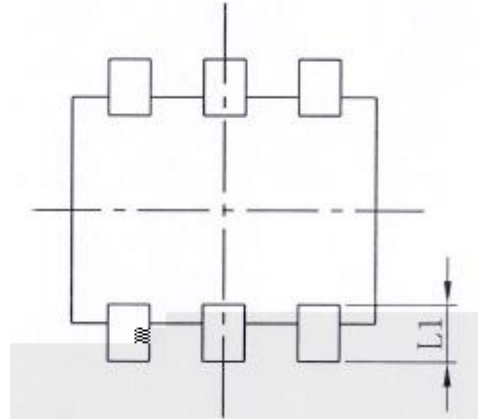
SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	-----		1.10
A1	0.000		0.10
A2	0.70		1.00
D	2.85		2.95
E	2.65		2.95
E1	1.55		1.65
b	0.30		0.50
c	0.08		0.20
e	0.95(BSC)		
L	0.30		0.60
	0°		8°

SCT2231

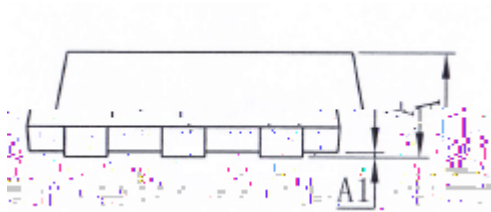
PACKAGE INFORMATION (SOT563)



SOT563 TOP VIEW



SOT563 BOTTOM VIEW



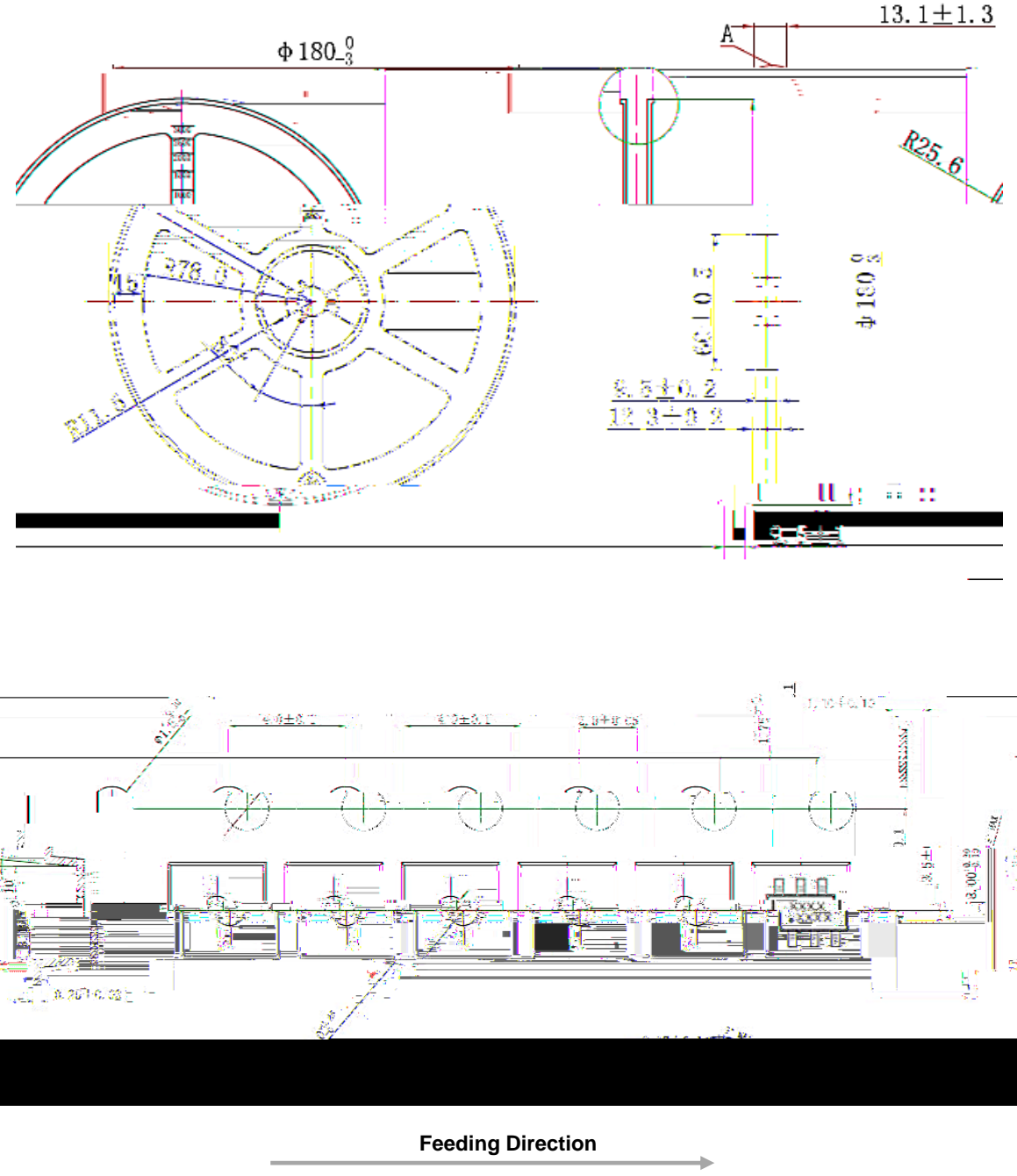
SOT563 SIDE VIEW

NOTE:

7. Drawing proposed to be made a JEDEC package outline MO-220 variation.
8. Drawing not to scale.
9. All linear dimensions are in millimeters.
10. Thermal pad shall be soldered on the board.
11. Dimensions of exposed pad on bottom of package do not include mold flash.
12. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.53		0.6
A1	0.000		0.05
b	0.19		0.27
b1	0.18	0.2	0.23
c	0.11		0.16
c1	0.1	0.11	0.12
D	1.5	1.6	1.7
E	1.5	1.6	1.7
E1	1.1	1.2	1.3
e	0.50BSC		
L	0.1	0.2	0.3
L1	0.2	0.5	0.4

TAPE AND REEL INFORMATION (TSOT23-6)



SCT2231

TAPE AND REEL INFORMATION (SOT563)

