

15W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

ED ST DR

- VIN Input Voltage Range: 4.2V-20V
- PVIN Input Voltage Range: 1V-20V
- Up to 15W Power Transfer
- Integrated Full-Bridge Power Stage with 17.5-m R_{ds(on)} of Power MOSFETs
- Integrated 5V-100mA LDO
- Optimized for EMI Reduction
- Build-in 3.3V-100mA LDO
- Integrated Lossless Input Current Sensor with ±2% accuracy for FOD and current Demodulation
- Integrated voltage and current demodulation
- Integrated Q factor detection
- 3.3V and 5V PWM Signal Logic Compatible
- Input Under-Voltage Lockout
- Over Current Protection
- Over Temperature Protection
- 3mm*3mm QFN-19L Package

OOKB SHNM

- WPC Compliant Wireless Chargers of 5W to 15W Systems for Mobiles, Tablets and Wearable Devices
- General Wireless Power Transmitters for Consumer, Industrial and Medical Equipment
- Proprietary Wireless Chargers and Transmitters

CDRB HSHNM

The SCT63142 is a highly integrated Power Management IC allows achieving high performance, high efficiency and cost effectiveness of wireless power transmitter system compliant with WPC specification to support up to 15W power transfer, working with a wireless application specific controller or a general MCU based transmitter controller.

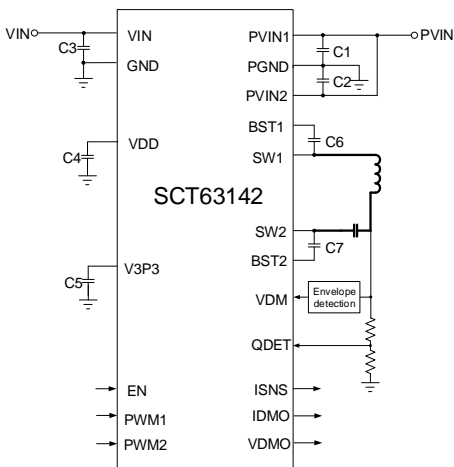
This device integrates a 4-MOSFETs full bridge power stage gate drivers, a 5V LDO, a 3.3V LDO, communication demodulator, Q-factor detection and input current sensor for both system efficiency and easy-to-use.

The proprietary gate driving scheme optimizes the performance of EMI reduction to save the system cost and design. The proprietary lossless current sensing circuitry with ±2% accuracy monitors input current of full bridge to support Foreign Object Detection FOD and current demodulation. The build-in 5V and 3.3V low dropout regulator LDO can provide power supplies to transmitter controller and external circuitries.

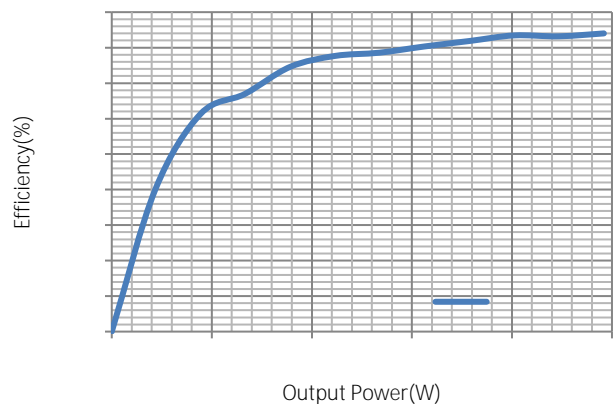
The SCT63142 features input Under-Voltage Lock-out UVLO, over current, short circuit protection, and over temperature protection.

The SCT63142 is available in a compact 3mm*3mm QFN package.

SXOHB K OOKB SHNM



On d S red Dech l d h s V W Unt s U



SCT63142

DUHNMGRSN X

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update EC

Revision 1.2: Update DEVICE ORDER INFORMATION

CDUHDN CD HMEN L SHM

**ORDERABLE
DEVICE**

VDD	6	Output voltage of the 5V LDO. Connect 2.2uF capacitor from this pin to GND pin. VDD is also the input power supply for gate driver of power stage and the 3.3V LDO.
V3P3	7	3.3V LDO output. Connect 2.2uF capacitor to ground.
QDET	8	Q-factor detection input.
VDM	9	High-pass filter input. Voltage demodulation pin data packets based on coil voltage.
BST2	10	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	11	Switching node of the half-bridge FETs Q3 and Q4.
SW1	12	Switching node of the half-bridge FETs Q1 and Q2.
BST1	13	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
VDMO	14	Voltage demodulation output
IDMO	15	Current demodulation output
ISNS	16	Current detection output. The voltage of the pin is proportional to the input current.
PWM2	17	PWM logic input to the FET Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q4, and turns on the high-side FET Q3. Logic LOW turns off the high-side FET Q3 and turns on the low-side FET Q4. When PWM input is in the tri-state mode, both Q3 and Q4 are turned off.
PWM1	18	PWM logic input to the FET Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q2, and turns on the high-side FET Q1. Logic LOW turns off the high-side FET Q1 and turns on the low-side FET Q2. When PWM input is in the tri-state mode, both Q1 and Q2 are turned off.
EN	19	Enable pin. Pull the pin high or keep it floating to enable the IC. When the device is enabled, IC will start to work if VIN higher than UVLO threshold. After VDD is established, power stage responds to PWM input logic then.

DBNL L DMC DC NOD SHMF BNMCHSHMR

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{IN}	Input voltage range	4.2	20	V
P _{VIN}	Input voltage range	1	20	V
T _J	Operating junction temperature	-40	125	°C

DRC SHMFR

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins ⁽¹⁾	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins ⁽²⁾	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

SGD L KHMEN L SHNM

PARAMETER	THERMAL METRIC	DFN-19L	UNIT
R	Junction to ambient thermal resistance ⁽¹⁾	48	°C/W
R	Junction to case thermal resistance ⁽¹⁾	45	

SCT63142

(1) SCT provides $R_{\theta JC}$ and $R_{\theta JA}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JC}$ and $R_{\theta JA}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63142 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63142. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JC}$ and $R_{\theta JA}$.

DKDBS HB KBG BSD HRS HBR

$V_{PVIN1}=V_{PVIN2}=12V$, $VDD=5V$, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
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V _{ISNS2}	Voltage with 1A input current	I _{PVIN} =1A, T _j =25	1.568	1.6	1.632	V
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Protection

T _{SD}	Thermal shutdown threshold	T _J rising	155	°C
	Hysteresis		35	°C

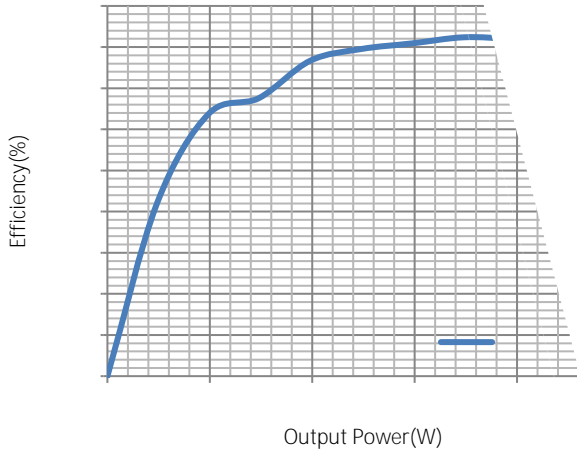


Figure 2. Transfer Efficiency with 5W RX@ Vout=5V

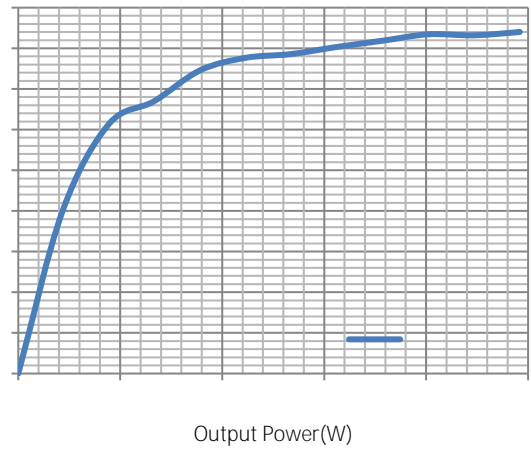


Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

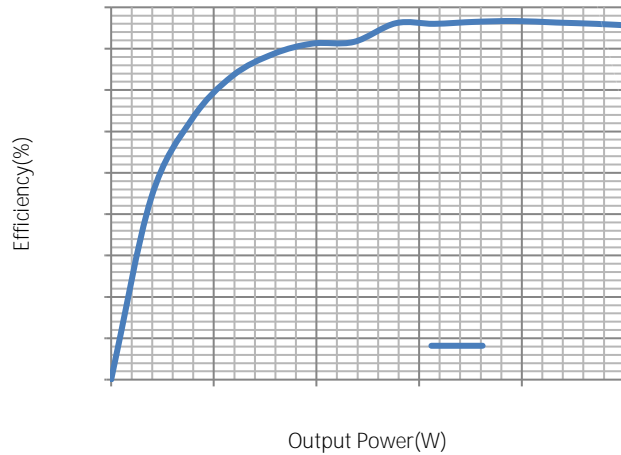


Figure 4. Transfer Efficiency with 15W RX@ Vout=12V

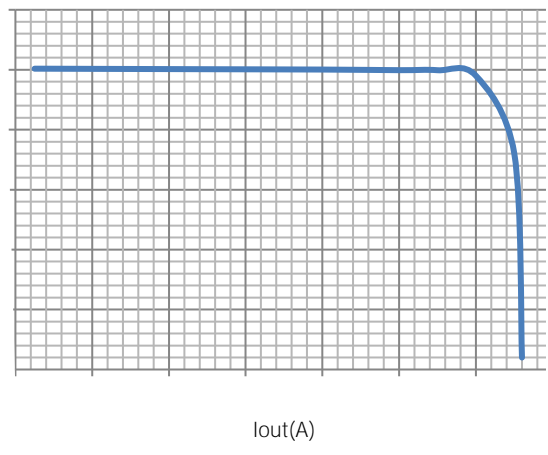


Figure 5. 5V LDO Iout vs Vout

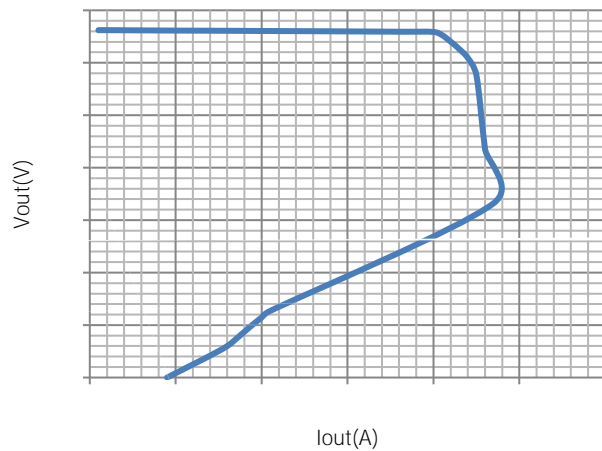


Figure 6. 3.3V LDO Iout vs Vout

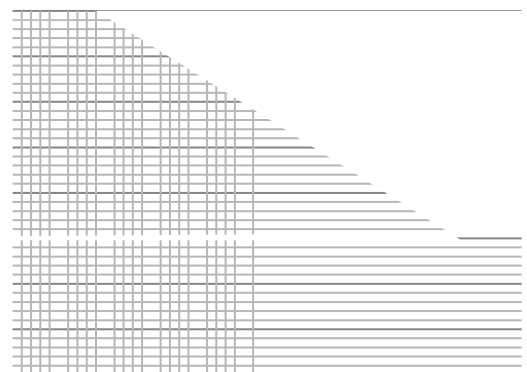


Figure 7. Current Sense Output Voltage vs Iin

ETMBSHM KAKNB CHF L

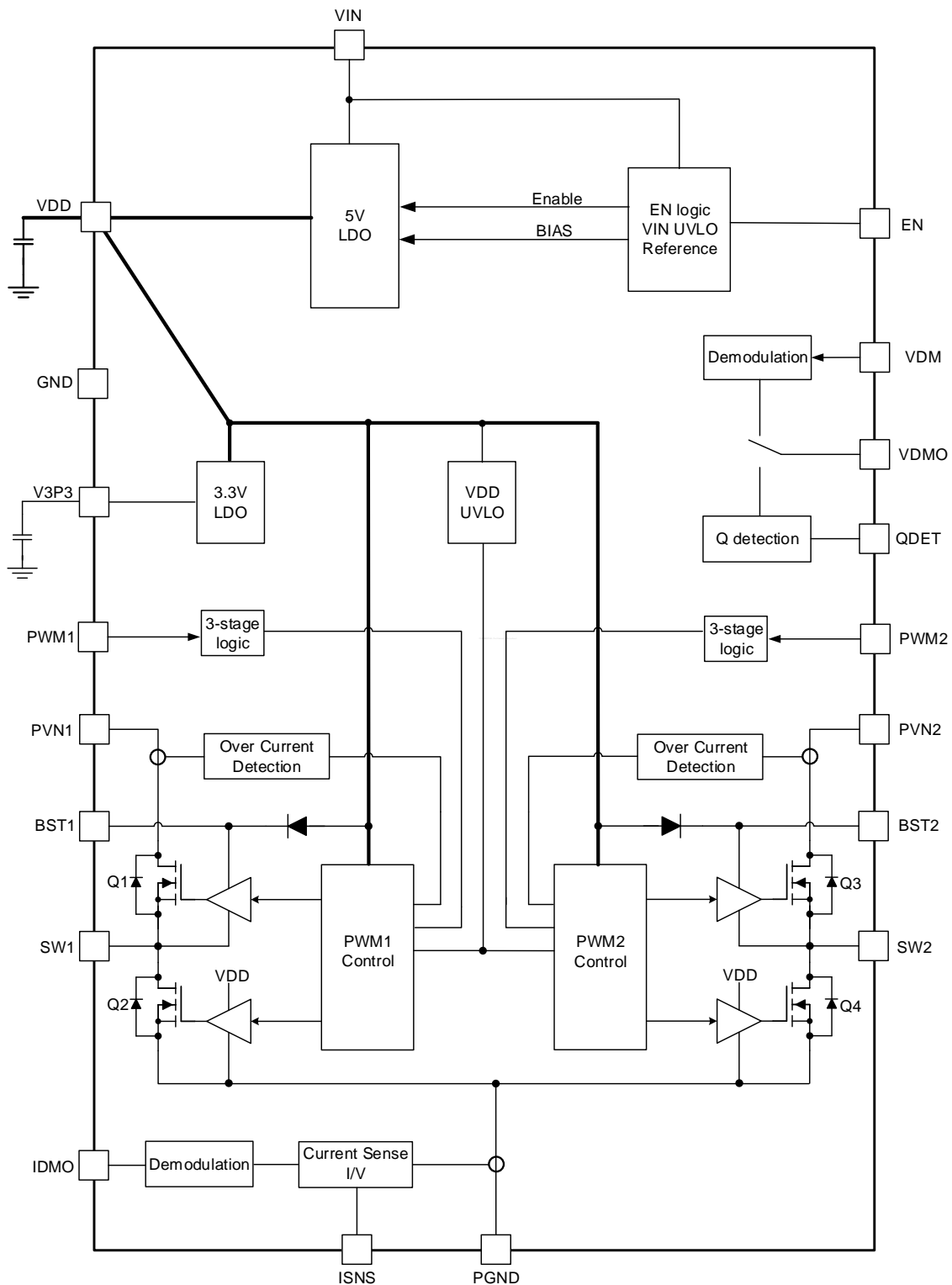


Figure 8. Functional Block Diagram

NOD SHM

Overview

The SCT63142 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V output LDO as power supply for external transmitter controller, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with $\pm 2\%$ accuracy, 3.3V output LDO for powering MCU.

The SCT63142 has three power input pins. VIN is connected to the power FETs of 5V LDO. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-Voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.08V typically. The maximum operating voltage for PVIN is up to 20V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63142 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63142 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for 4-MOSFETs full bridge, current limit and current fold back at hard short for two LDOs and whole chip thermal shutdown protection.

Enable and Start up Sequence

When the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.18V, the 5V output LDO enables at once. And the device disables when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.1V. VDD ramp up after 5V LDO works, and also the V3V. Once VDD rise up to 3.8V and V3V is higher than 3V, 4-MOSFETs full bridge allows PWM signal to control for switching. PWM input cannot control full bridge of MOSFETs if VDD drop to 3.36V or V3V drop to 2.7V.

An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin is floating to simply the system design. If an application requires a higher system under voltage lockout threshold, two external resistors divider (R1 and R2) in Figure 9 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{\text{rise}} = 1.18 \left(1 + \frac{R1}{R2} \right) - 1.5\mu\text{A} \cdot R1 \quad (1)$$

$$V_{\text{fall}} = 1.1 \left(1 + \frac{R1}{R2} \right) - 5.5\mu\text{A} \cdot R1 \quad (2)$$

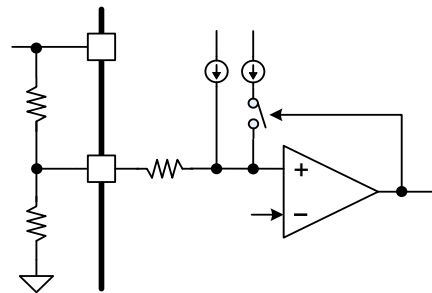


Figure 9. System UVLO by enable divider

5V LDO

The SCT63142 has an integrated low-dropout voltage regulator which powered from VIN and supply regulated 5V voltage on VDD pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of external transmitter controller directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VDD pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Full bridge and PWM Control

The SCT63142 integrate full bridge power stage with only 16mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 20KHz to 400KHz for different applications which is completely compatible with WPC's frequency requirement from 100KHz to 205KHz.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

PWM1 and PWM2 also support tri-state input. When PWM input logic first enters tri-state either from logic HIGH or logic LOW, the states of its controlled FETs stay the same. If the PWM input stays in the tri-state for more than 60ns, its controlled FETs are all turned off, and the corresponding SW output becomes high impedance. The FETs stay off until the PWM logic reaches logic HIGH or logic LOW threshold.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot be kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

Full Bridge Over Current Protection

The SCT63142 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 9.5A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

Current Sense

The SCT63142 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with $\pm 2\%$ accuracy and reports a proportional voltage directly to the ISNS pin. This voltage information on ISNS pin can be send to specialized controller or general MCUD 165/Lang (en-US)BDC q0.000009m0 G(or)

SCT63142

3.3V LDO

The SCT63142 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Q Factor Detection

The SCT63142 integrated a low cost, reliable Q factor detection circuit to assure foreign objects detection before the selection phase. It generates a small pulse to detect any foreign object on the transmitter coil, it can detect metal on the transmitter coil easily.

After chip enable, apply a low voltage level pulse to EN pin can trigger the Q factor detection feature. The pulse width should be longer than 50us but less than 200us. SW1 will be preset to 2V for 4.7ms and then pull low to ground and this apply power to LC resonant loop and Vcoil will appear damping oscillation after SW1 short to ground. The SCT63142 will generate a pulse on VDMO pin and MCU can capture this pulse to calculate the Q factor by the pulse width as the Equation 4 shows. PWM1 and PWM2 should be low in Q factor detection phase.

Thermal Shutdown

The SCT63142 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155C, the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120C, then the device restarts.

OOKIB SHMHMEN L SHM

Typical Application

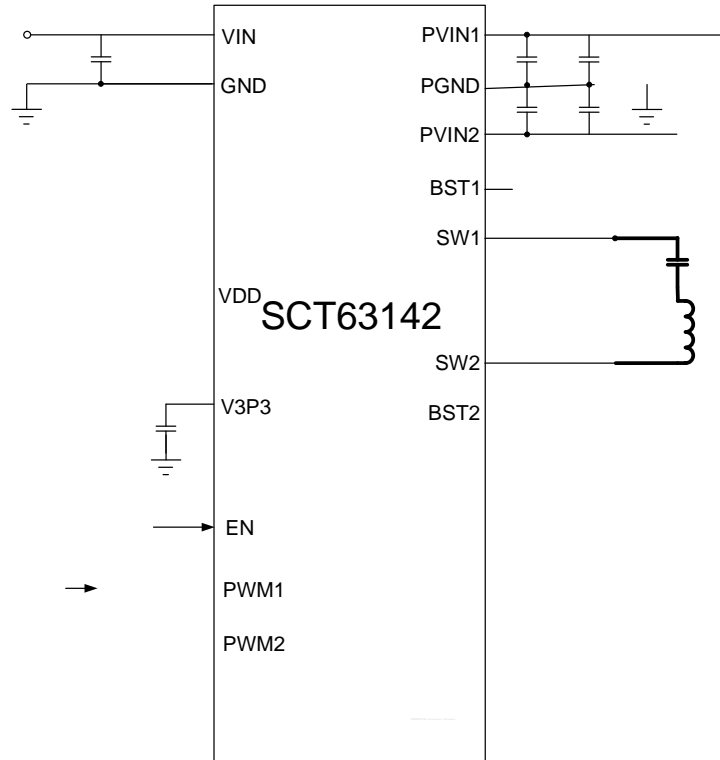


Figure 11. Same Input to VIN and PVIN

Application Waveforms

Figure 12. Power Up

Figure 13. Power Up

Figure 14. Power Down

Figure

Layout Guideline

Proper PCB layout is a critical for SCT63142 guidelines as below:

For better results, follow these

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Bypass capacitor for VDD place next to VDD pin.
5. Bypass capacitor for V3V place next to V3V pin.

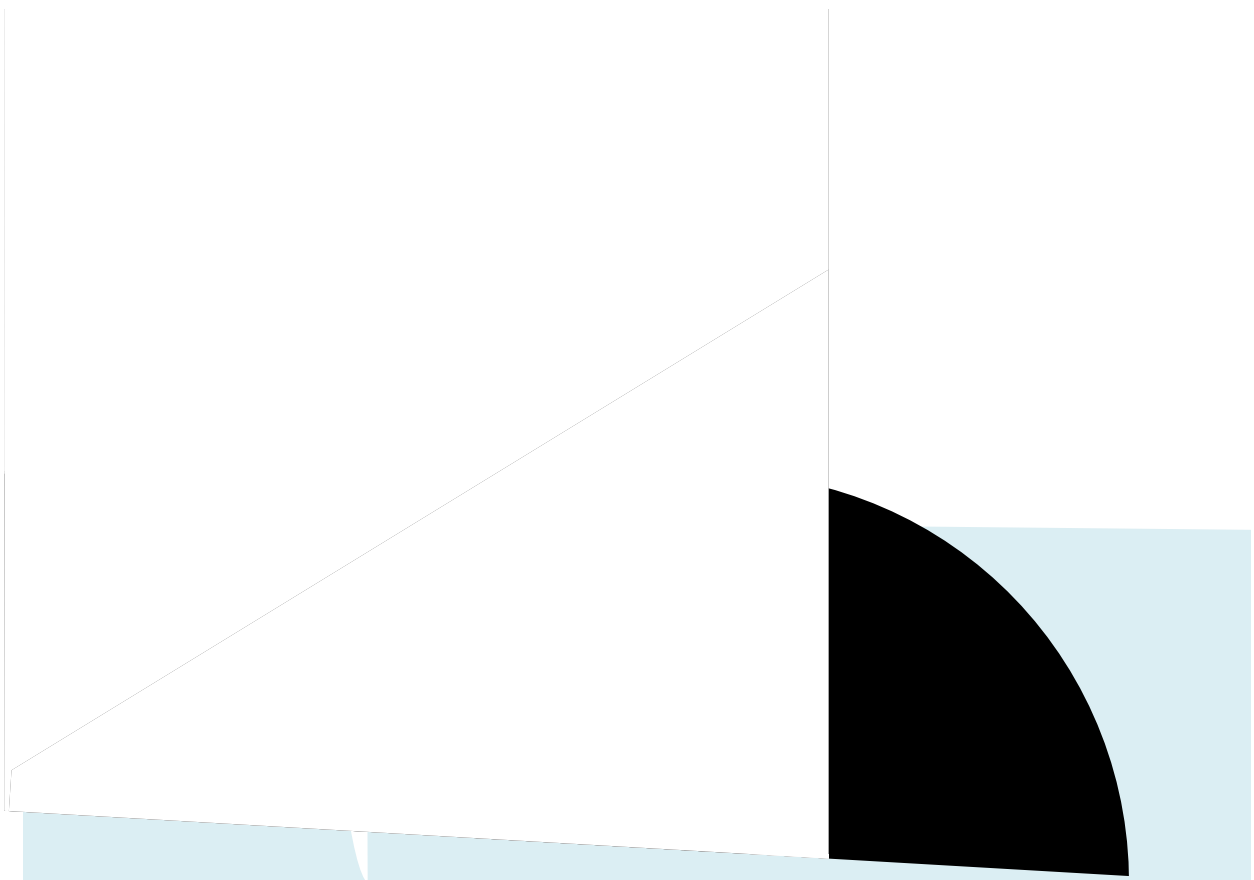
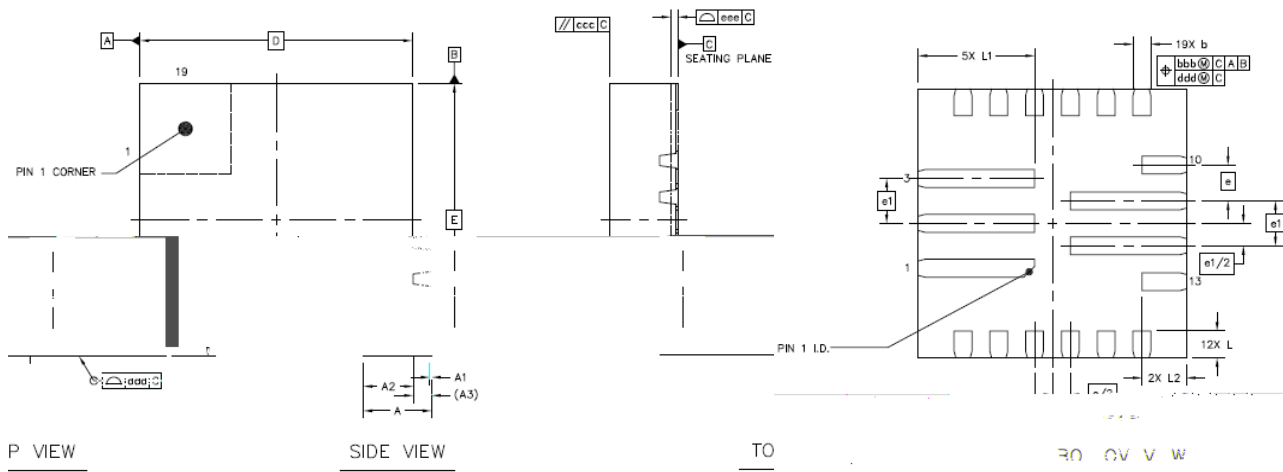


Figure 18. PCB Layout Example

O B F D H M E N L S H M



FCQFN-19L (3x3) Package Outline Dimensions

	Symbol	Dimensions in Millimeters		
		Min.	Nom.	Max.
TOTAL THICKNESS	A	0.70	0.75	0.80
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE	X	D		
	Y	E		
LEAD PITCH	e	0.40 BSC		
	e1	0.50 BSC		
LEAD LENGTH	L	0.20	0.30	0.40
	L1	1.2	1.3	1.4
	L2	0.4	0.5	0.6
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
COPLANARITY	eee	0.08		
LEAD OFFSET	bbb	0.1		
	ddd	0.05		

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

S OD MC DDKHMEN L SHNM

