3.8V

- EMI Reduction with Switching Node Ringing-free
- 500kHz Switching Frequency with 6% Frequency Spread Spectrum FSS
- Pulse Skipping Mode PSM with 20uA Quiescent Current in Light Load Condition
- 3.8V-32V Wide Input Voltage Range
- Up to 2A Continuous Output Load Current
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 130 R_{dson} High Side MOSFET and 70 R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Dropout Mode Operation
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in SOP-8L Package

- White Goods, Home Appliance
- Surveillance
- Audio, WiFi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display

The SCT9320 is 2A, 500KHz, synchronous buck converter with up to 32V

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to Market

Revision 1.1: Update description in Typical Application

Revision 1.2: Format adjustment

Revision 1.3: Update Device Order Information

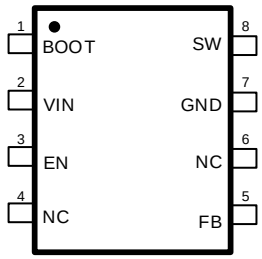
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT9320STDR	Tape & Reel	4000	9320	8	SOP-8L

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	40	V
VIN, SW, EN	-0.3	34	V
FB	-0.3	5.5	V
Operating junction temperature TJ(2)	-40	125	°C
Storage temperature TSTG	-65	150	°C

(1)

(2)



Top View: SOP-8L, Plastic

NAME	NO.	PIN FUNCTION
BOOT	1	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
VIN	2	Power supply input. Must be locally bypassed.
EN	3	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.18V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
FB	5	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.

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NC	4, 6	Not connected.
GND	7	Power ground. Must be soldered directly to ground plane.
SW	8	Switching node of the buck converter.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	32	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER

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V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						

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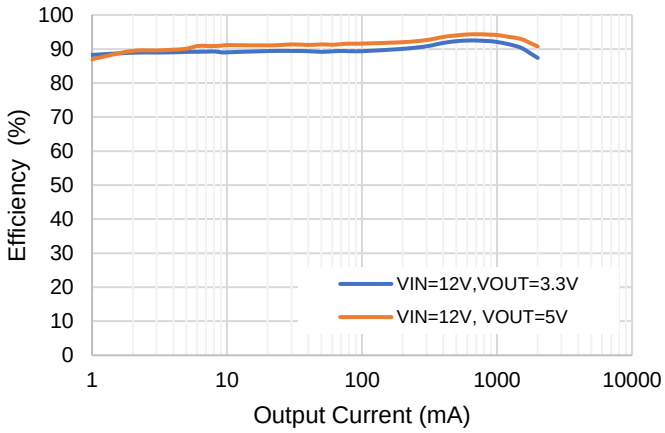

Figure 1. SCT9320 Efficiency, Vin=12V

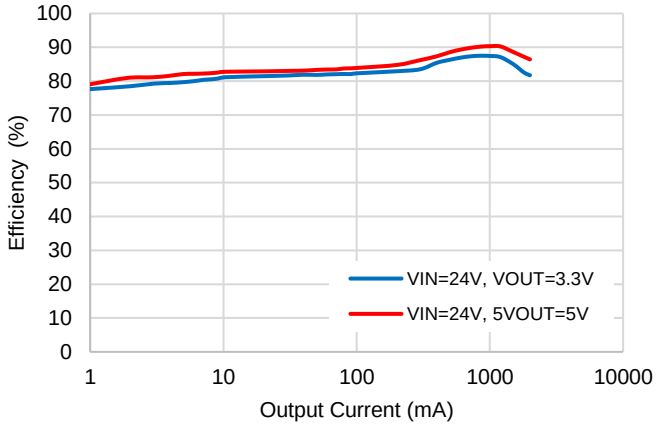

Figure 2. SCT9320 Efficiency, Vin=24V

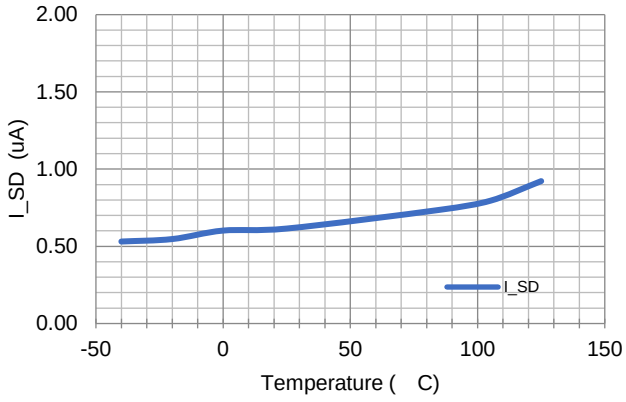

Figure 3. Shut-down Current vs Temperature

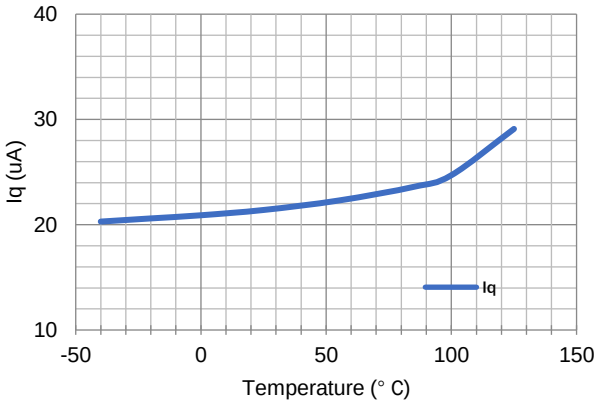

Figure 4. Quiescent Current vs Temperature

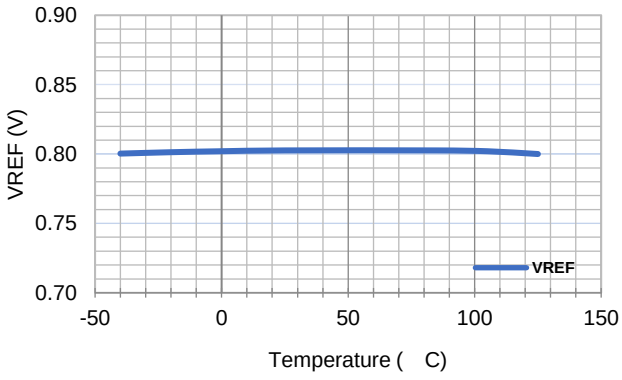

Figure 5. Reference Voltage vs Temperature

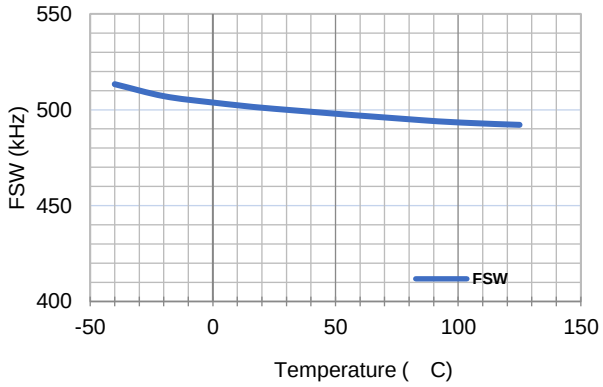

Figure 6. Center Switching Frequency vs Temperature

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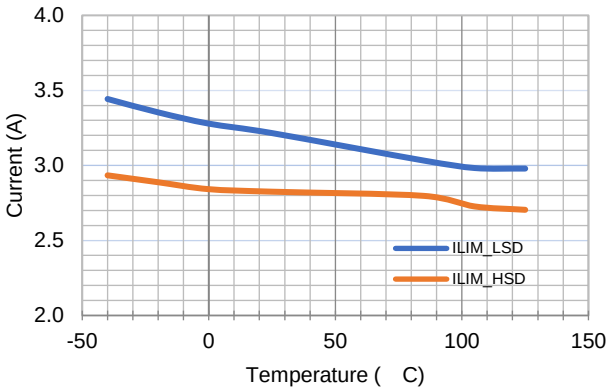

Figure 7. Peak Current Limit vs Temperature

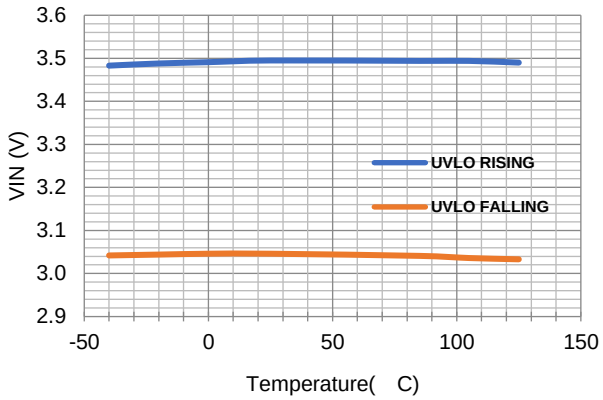

Figure 8. VIN UVLO vs Temperature

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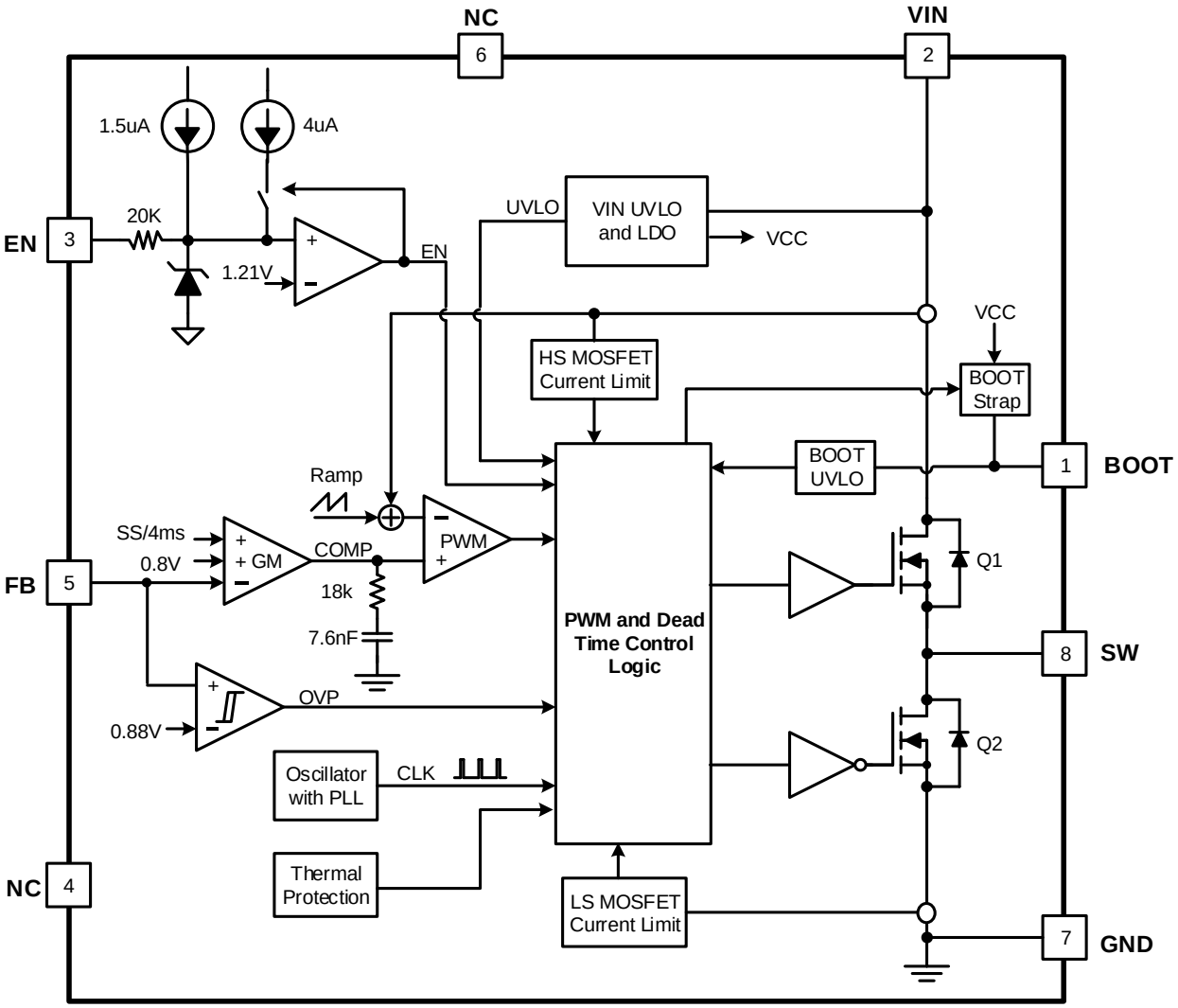
NC
6
VIN
2
1.5uA
4uA
20K
EN
3
1.21V
EN
UVLO
VIN UVLO
and LDO
VCC
VCC
HS MOSFET
Current Limit
BOOT
Strap
BOOT
UVLO
1
BOOT
Ramp
SS/4ms
0.8V
FB
5
+ GM
COMP
PWM
18k
7.6nF
PWM and Dead
Time Control
Logic
Q1
8
SW
OVP
0.88V
Q2
Oscillator
with PLL
CLK
Thermal
Protection
LS MOSFET
Current Limit
NC
4
7
GND

Overview

The SCT9320 device is 3.8V-32V input, 2A output, EMI friendly, fully integrated synchronous buck converter. The device employs fixed frequency peak current mode control. An internal clock with 500kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 4ms soft-start simplify the SCT9320 footprints and minimize the off-chip component counts.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The quiescent current of SCT9320 is 20uA typical under no-load condition and no switching. When disabling the device, the supply shut down current is only 1 The SCT9320 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition, hence the power efficiency can be achieved up to 88% at 5mA load condition.

The SCT9320 implements the Frequency

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and the device starts soft-start phase. The SCT9320 has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 9. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

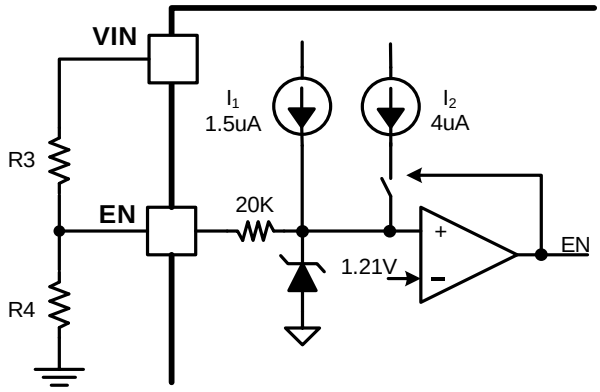

Figure 9. Adjustable VIN UVLO

(1)

(2)

Where:

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1.5uA
I_2=4uA
V_{ENR}=1.18V
V_{EMF}=1.1V

EMI Reduction with Frequency Spread Spectrum and Switching Node Ringing-free

In some applications, the system EMI test must meet EMI standards EN55011 and EN55022. To improve EMI performance, SCT9320 adopts Frequency Spread Spectrum (FSS) to spread the switching noise over a wider band and therefore reduces conducted and radiated interference peak amplitude at particular frequency. The SCT9320 features 500kHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching

frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency from fixed 500kHz to a range 517kHz ~ 583kHz. As a result, the harmonic wave amplitude is reduced and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT9320 implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design). The switching node zoomed in wave form is shown in Figure 10.

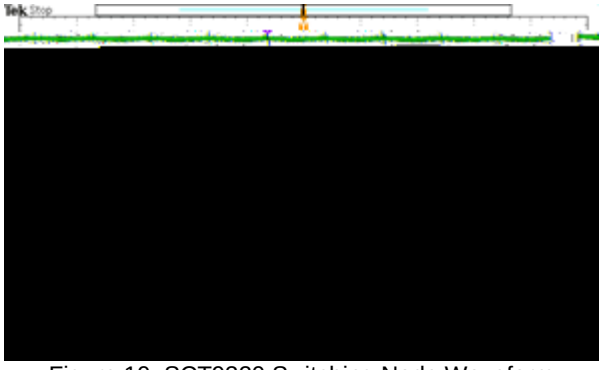

Figure 10. SCT9320 Switching Node Waveform

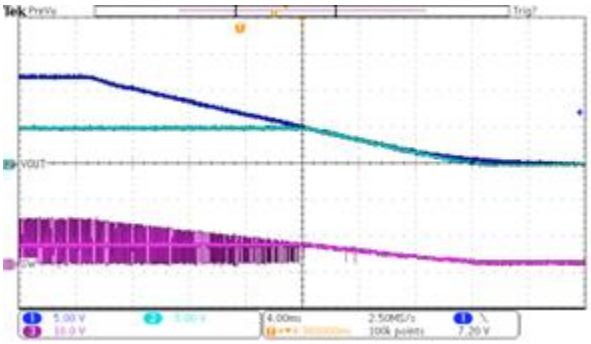

Figure 11. SCT9320 LDO Mode Waveform

Peak Current Limit and Hiccup Mode

The SCT9320 has cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on,

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to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT9320 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-out Regulation

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT9320. The Low Drop Out Operation is triggered automatic when the off time of the high-side power MOSFET exceeds the minimum off time limitation.

In low drop out operation, high-side MOSFET remains ON as long as the BST pin to SW pin voltage is higher than BST UVLO threshold. When the voltage from BST to SW drops below 2.35V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Only 100ns of low side MOSFET turning on in each refresh cycle minimizes the output voltage ripple. Low-side MOSFET may turn on for several times till bootstrap voltage is charged to higher than 2.7V for high-side

MOSFET working normally. Then high-side MOSFET turns on and remains on until bootstrap voltage drops to

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Typical Application

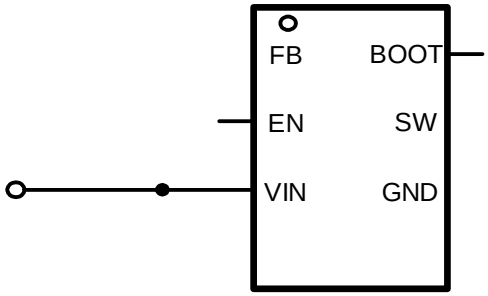

Figure 12. 24V Input, 5V/2A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	24V
Output Voltage	5V
Output Current	2A
Output voltage ripple (peak to peak)	±0.3V
Switching Frequency	500kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 recommended for the decoupling capacitor anda0.1 to be placed as close as possible to the VIN pin of the SCT9320.

Use Equation (3) to calculate the input voltage ripple:

(3)

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of e operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

(4)

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation (5).

(5)

Set the current limit of the SCT9320 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core

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- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

(9)

Output Feed-Forward Capacitor Selection

The SCT9320 has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c. Equation (10) is used to calculate the feed-forward capacitor.

(10)

Output Feedback Resistor Divider Selection

The SCT9320 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure12. Use equation (11) to calculate the resistor divider values.

(11)

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.

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Application Waveforms

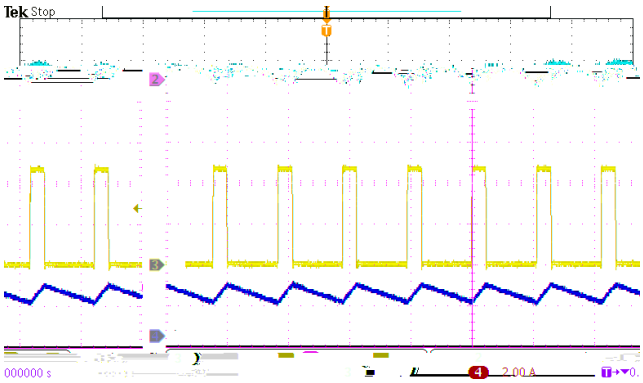

Figure 13. SW node waveform and Output Ripple
VIN=24V, IOUT=2A

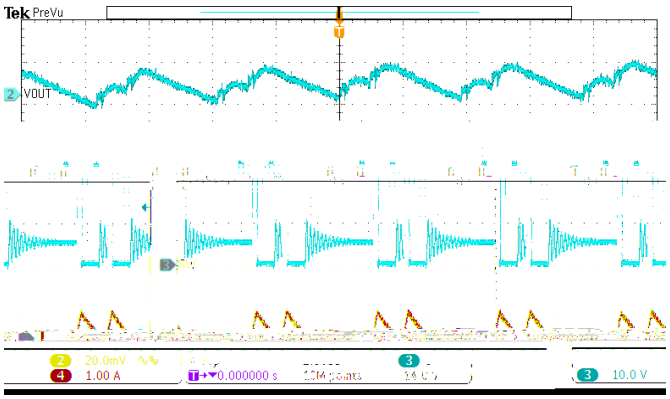

Figure 14. SW node Waveform and Output Ripple
VIN=24V, IOUT=100mA

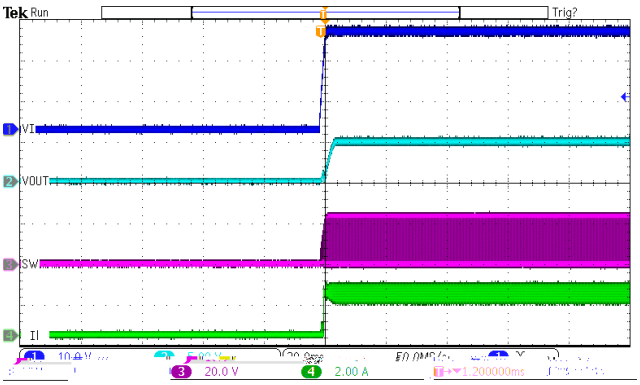

Figure 15. Power Up
VIN=24V, VOUT=5V, IOUT=2A

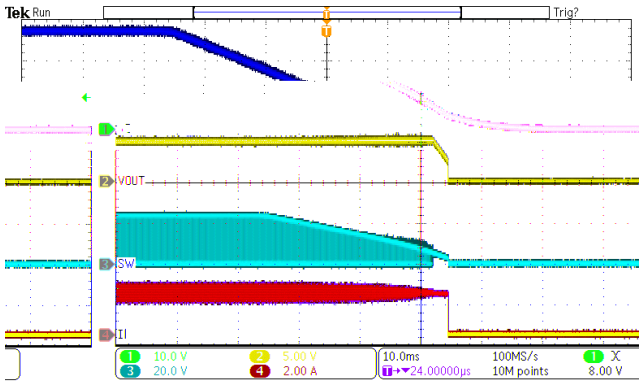

Figure 16. Power Down
VIN=24V, VOUT=5V, IOUT=2A

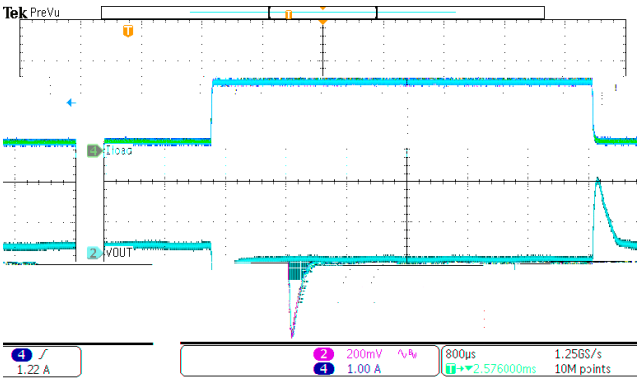

Figure 17. Load Transient
VOUT=5V, IOUT=0.2A to 1.8A, SR=250mA/us

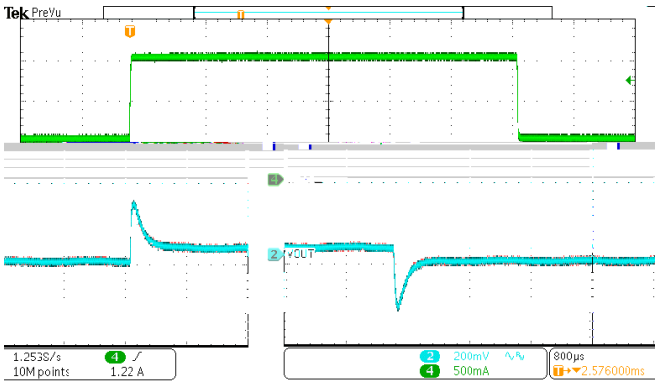

Figure 18. Load Transient
VOUT=5V, IOUT=0.5A to 1.5A, SR=250mA/us

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Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 19 is the recommended PCB layout of SCT9320.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

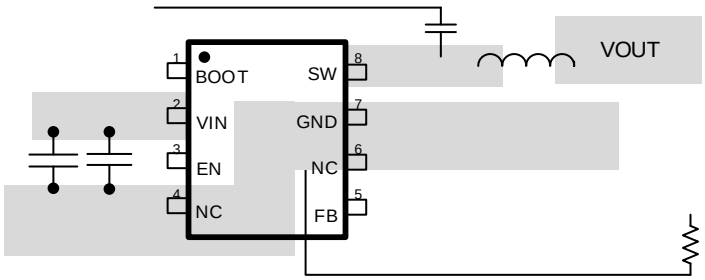

Figure 19. PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (12).

(12)

where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

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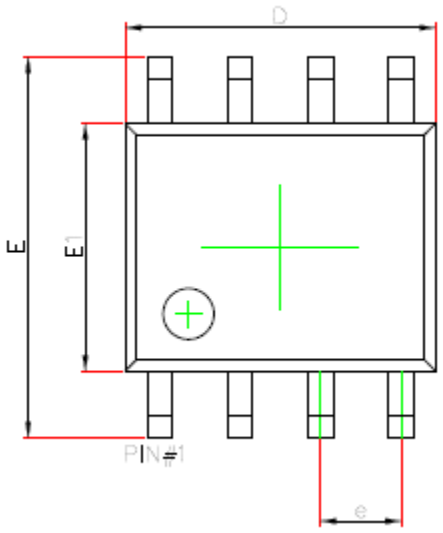
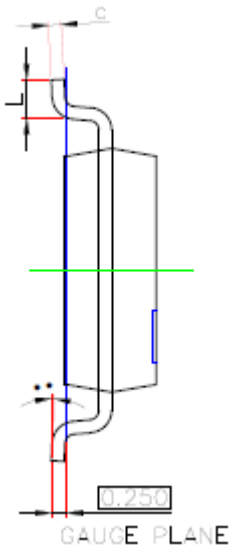
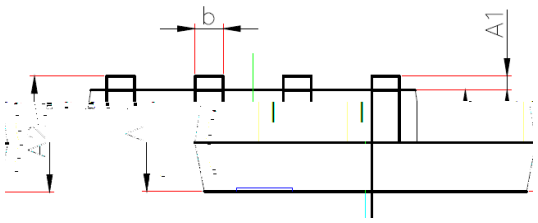


TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.35		1.75
A1	0.1		0.25
A2	1.35		1.55
D	4.8		5
E	5.8		6.2
E1	3.8		4.0
b	0.33		0.51
c	0.17		0.25
e	1.27(BSC)		
L	0.40		1.27
	0		8

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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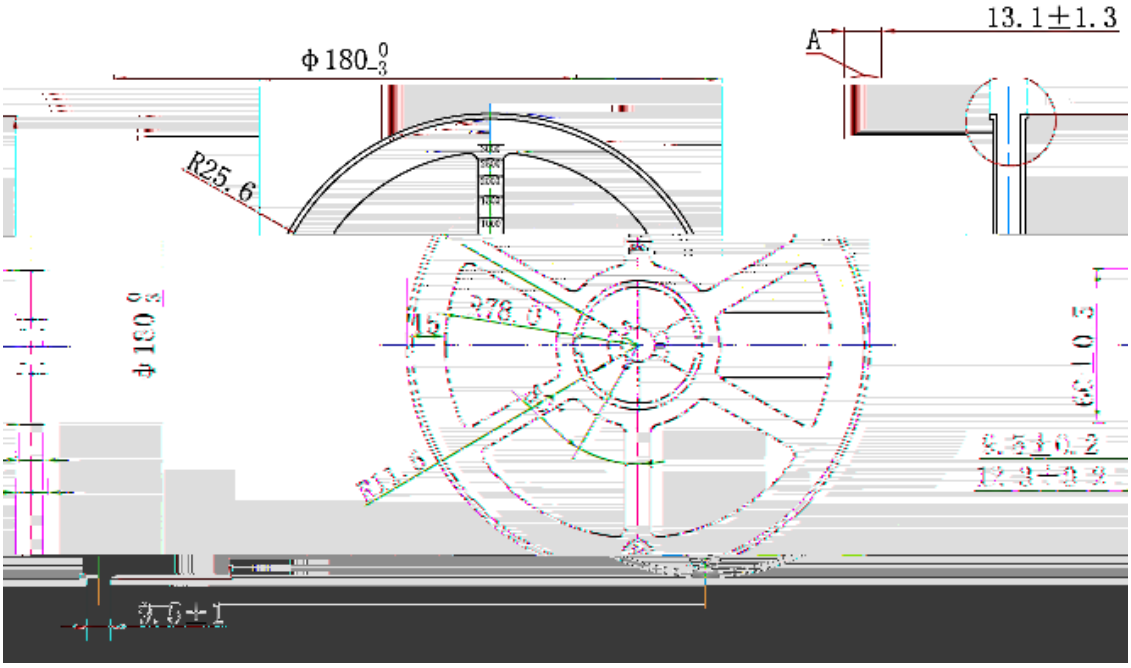

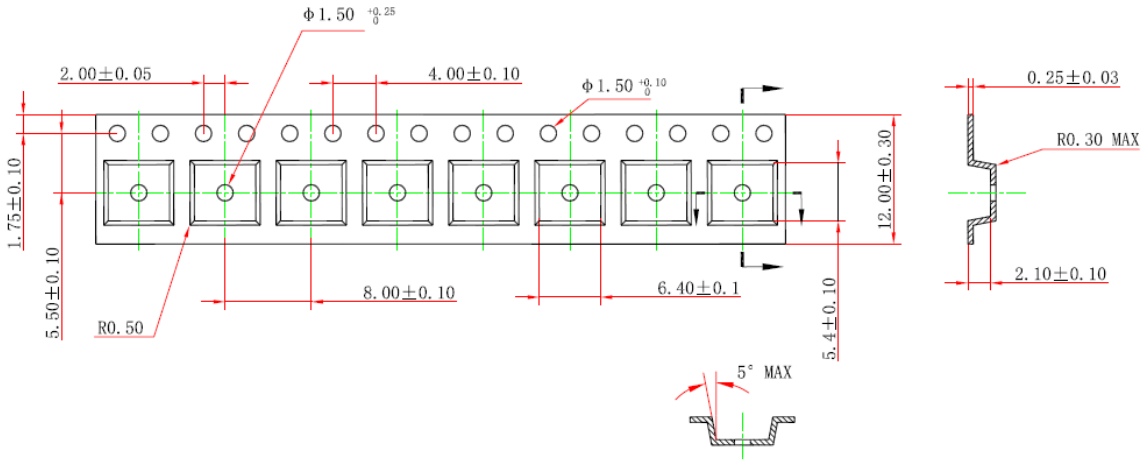

Feeding Direction

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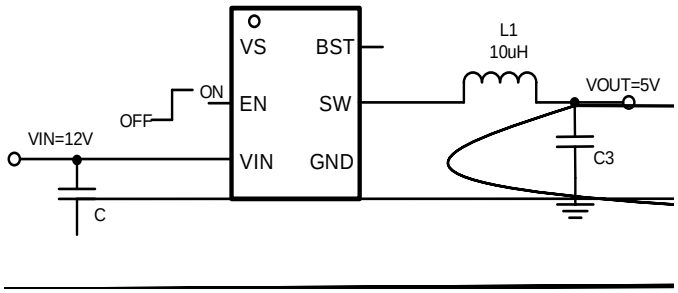
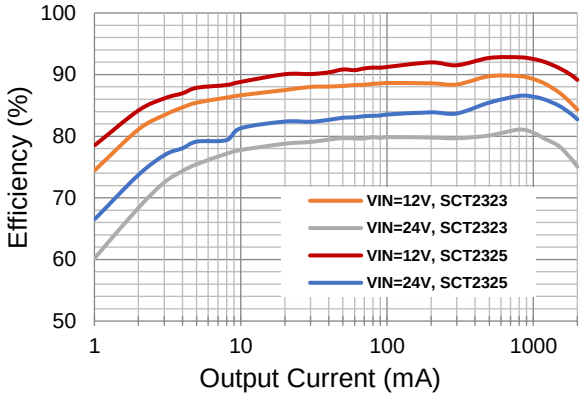
24V Vin, 5V Vout, 1.1MHz Synchronous Buck Converter



Power Efficiency



PN	DESCRIPTION	COMMENTS
SCT2325 **SCT2323**	3.8V-32V Vin, Fixed Vout, 2A Synchronous Buck Converter with EMI Reduction	• 1.1MHz switching frequency with ±6% FSS • EMI reduction with switching node ringing-free. • SW anti-ringing in discontinuous current mode • 20uA ultra-low quiescent current • Minimum external components. Easy-to-use • Fixed 5V Vout (SCT2325) and 3.3V Vout (SCT2323)
SCT2330 **SCT2331**	3.8V-32V Vin, 3A Synchronous Step-down DCDC Converter with EMI Reduction	• 500KHz switching frequency • 3A Continuous output current • EMI reduction with switching node ringing-free. • Ultra-low quiescent current. High efficiency PFM at light load (SCT2330) • Frequency Spread Spectrum (SCT2330) • Fixed PWM mode for lower output ripple (SCT2331)

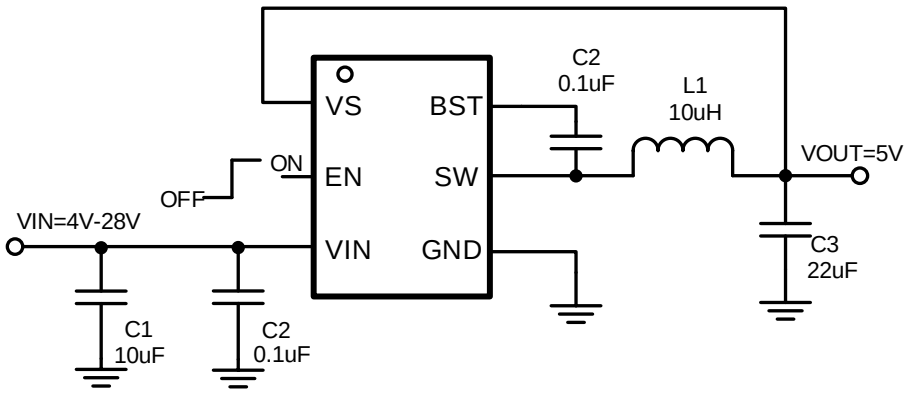


Figure 20. SCT2325 Typical Application

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