REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.4: Update DEVICE ORDER INFORMATION

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT12A2DHKR	Tape & Reel	3000	12A2	20	20-Lead 3.5mm×4.5mm Plastic QFN

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	28	V
VIN, SW, VOUT, FSW, PGATE	-0.3	22	V
VCC, LIM FB EN,SS, COMP, MODE	-0.3	5.5	V
Operating junction temperature T_J(2)	-40	125	C
Storage temperature T_{STG}	-65	150	C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150℃ when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

PIN CONFIGURATION

Top View: 20-Lead Plastic DFN 3.5mmx4.5mm

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
VCC	1	Internal linear regulator output. Connect a 1uF or larger ceramic capacitor to ground. VCC cannot to be externally driven. No additional components or loading is recommended on this pin.
EN	2	Enable logic input. A 8 connects this pin to ground inside. Floating disables the device.
FSW	3	Place a resistor from this pin to SW to set the switching frequency.
SW	4,5,6,7	Switching node of the boost converter.
BOOT	8	Power supply for the high-side FET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
VIN	9	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
SS	10	Place a ceramic cap from this pinto ground to program soft-start time. An internal 5uA current source pulls SS pin to VCC.
NC	11	Not Connected.
MODE	12	Ground connected enables PSM mode.
PGATE	13	Gate driver output for an external P-channel MOSFET to disconnect load.

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VOUT	14,15,16	Boost converter output. Connect a 1uF decoupling capacitor as close to VOUT pins and power ground pad as possible to reduce the ringing voltage of SW.
FB	17	Feedback Input. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference value of 1.2V typical.
COMP	18	Output of the error amplifier and switching converter loop compensation point.
ILIM	19	Inductor peak current limit set point input. A resistor connecting this pinto ground sets current limit through low-side power FET.
AGND	20	Analog ground. Analog ground should be used as the common ground for all small signal analog inputs and compensation components. No electrical connection to PGND inside.
PGND	21	Power ground. Must be soldered directly to ground planes using multiple vias directly under the IC for improved1ET 58.2 Q EMC /Span <</MCID 75/Lang (en-U

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, T_J=-40℃ ~125℃ , typical values are tested under 25℃ .

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		20	V
V_{OUT}	Output voltage range		4.5		21	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.6 200	2.7	V mV
I_{SD}	Shutdown current	EN=0, no load and measured on VIN pin		1	3	uA
I_Q	Quiescent current from VIN	EN=2V, no load, no switching		1		uA
	Quiescent current from VOUT			420		uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.8		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB	FPWM mode	1.180	1.206	1.230	V
		PSM mode	1.196	1.220	1.244	V
I_{FB}	FB pin leakage current	V_{FB}=1.2V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		200		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		20		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		20		uA
V_{COMP_H}	COMP high clamp	V_{FB}=1V R_{ILIM}		1.5		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.5V, R_{ILIM} M		0.6		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			13		
R_{DSON_L}	Low side FET on-resistance			11		
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}		15		A
Enable and Mode						
V_{EN}	Enable high threshold Enable low threshold	V_{CC}=5V	 0.4		1.2	V V
R_{EN}	Enable pull down resistance			800		
V_{MODE}	MODE high threshold MODE low threshold	V_{CC}=5V	 1.5		4	V V
I_{SS}	Soft-start charging current			5		uA
Switching Frequency						
F_{SW}	Switching frequency	R_{FSW}=301k, V_{OUT}=12V		520		kHz
t_{ON_MIN}	Minimum on-time	R_{FSW}=301k, V_{OUT}=12V		160	200	ns
t_{OFF_MIN}	Minimum off-time	R_{FSW}=301k, V_{FB}=0V		480	150	ns
Load Disconnection Control						
I_{PGATE}	PGATE pull down current			250		uA
V_{PGATE_C}	Clamp voltage between PGATE and VOUT			6.1	7	V
Protection						
V_{OVP_VOUT}	Output overvoltage threshold	V_{OUT} rising		22		V

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
	Hysteresis			400		mV
V_{OVP_VFB}	Feedback overvoltage with respect to reference voltage	V_{FB} rising V_{FB} falling		110 105		% %
T_{SD}	Thermal shutdown threshold	T_J rising		150		℃
	Hysteresis			20		℃

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TYPICAL CHARACTERISTICS

Figure 1. Efficiency, Vout=12V, fsw=400KHz, PFM

Figure 2. Efficiency, Vout=15V, fsw=400KHz, PFM

Figure 3. Efficiency, fsw=400 kHz, 1-cell Battery, PFM

Figure 4.

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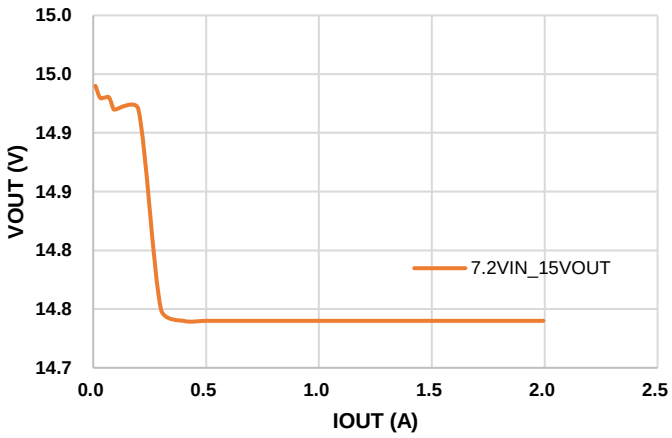

Figure 7. Load Regulation (Vin=7.2V, Vout=15V)

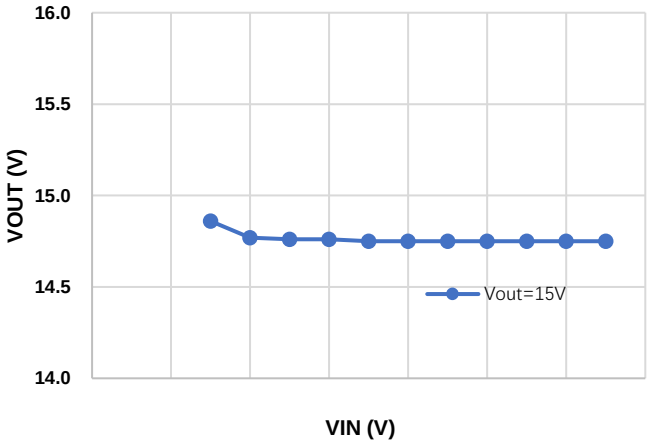

Figure 8. Line Regulation (Vout=15V)

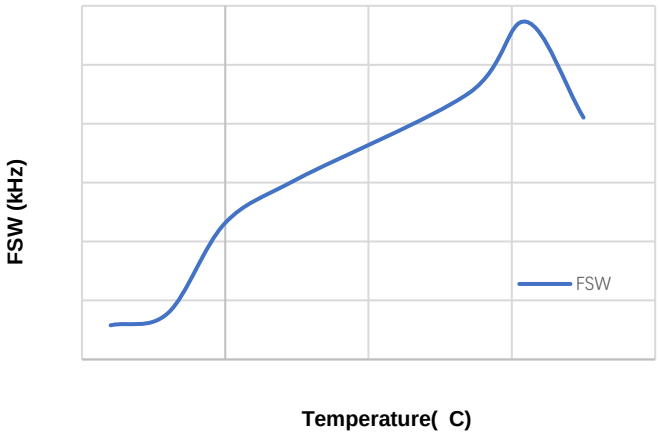

Figure 9. Frequency vs Temperature

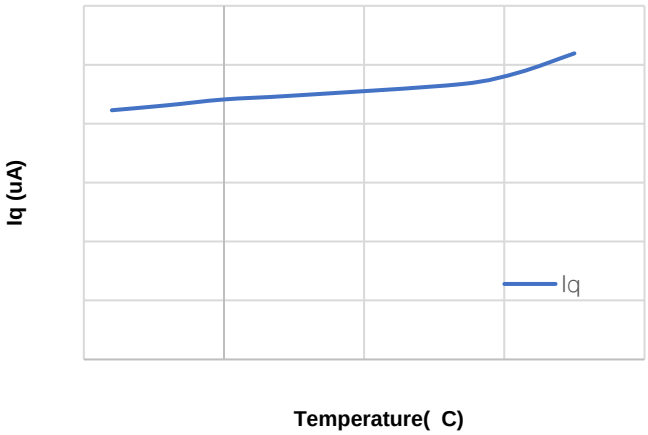

Figure 10. Quiescent Current vs Temperature

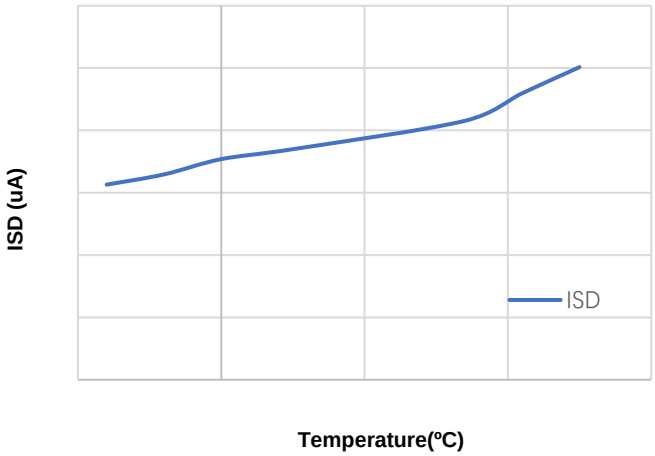

Figure 11. Shutdown Current vs Temperature

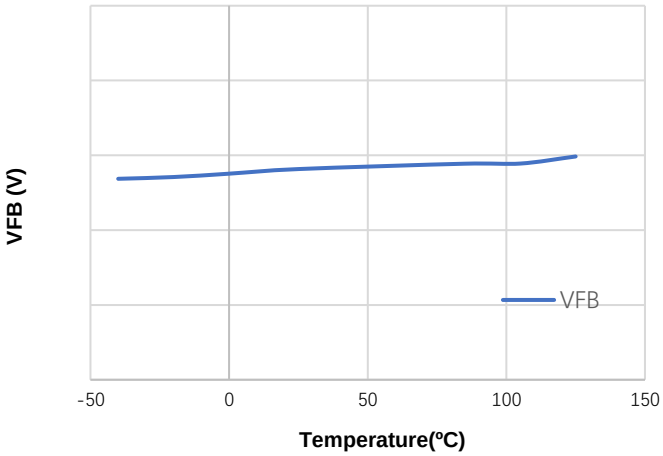

Figure 12. Feedback Reference vs Temperature

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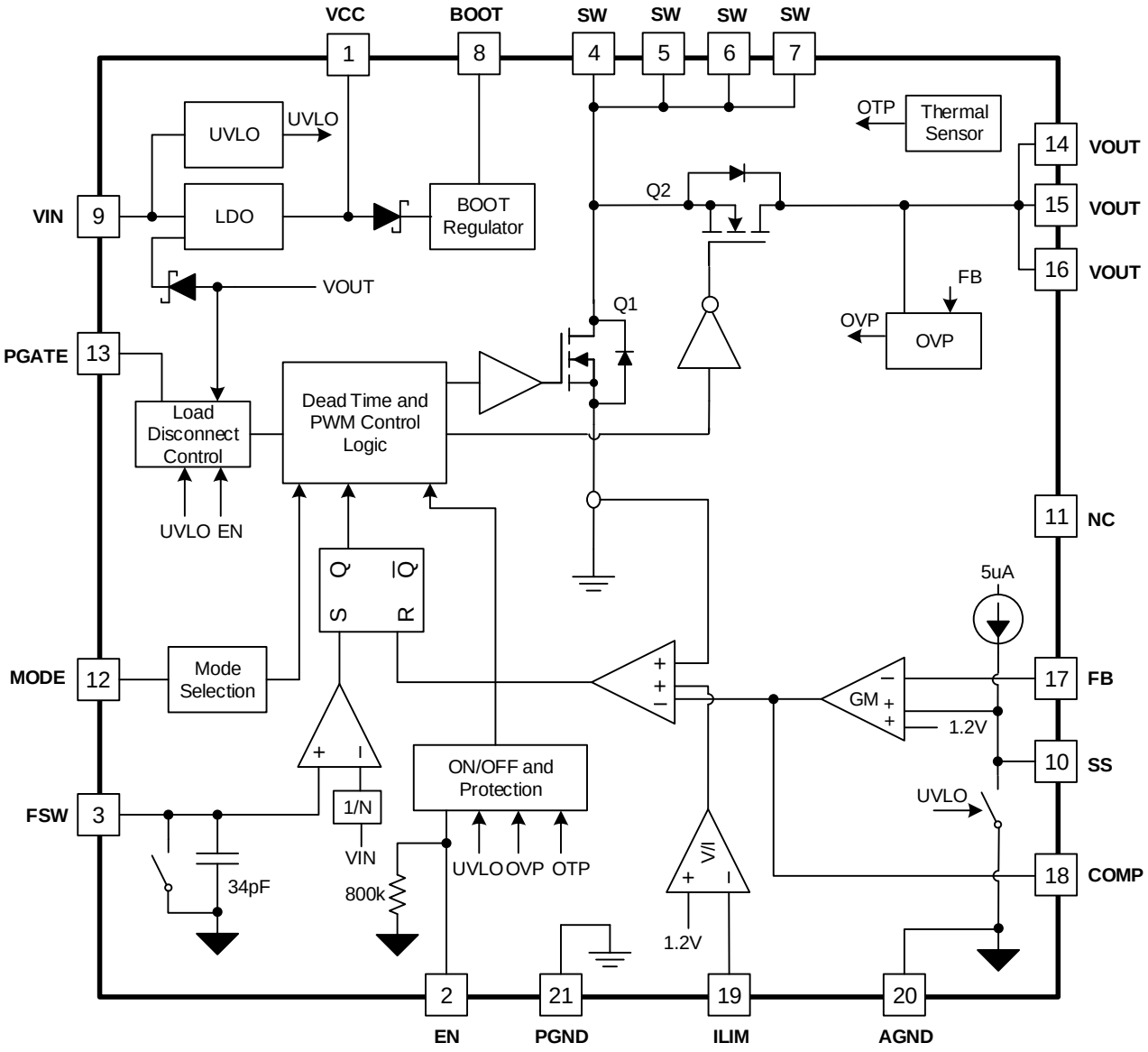
FUNCTIONAL BLOCK DIAGRAM



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OPERATION

Overview

The SCT12A2 device is a fully integrated synchronous boost converter, which regulates output voltage higher than input voltage. The constant off-time peak current mode control provides fast transient with pseudo fixed switching frequency. When low-side MOSFET Q1 turns on, input voltage forces the inductor current rise. Sensed voltage on low-side MOSFET peak current rises above the voltage of COMP. After the inductor current reaches the peak current, the device turns off low-side MOSFET and inductor goes through body diode of high-side MOSFET Q2 during dead time. After dead time duration, the device turns on high-side MOSFET Q2 and the inductor current decreases. Based on Vin and Vout voltage, the device predicts required off-time and turns off high-side MOSFET Q2.This repeats on cycle-by-cycle based.

The voltage feedback loop regulates the FB voltage to a 1.2V reference with an internal trans-conductance error amplifier. The feedback loop stability and transient response are optimized through an external loop compensation network connected to the COMP pin.

When MODE pin is connected to ground, the SCT12A2 works at PFM mode to further increase the efficiency in light load condition. The quiescent current of SCT12A2 is 420uA typical under no-load condition and not switching. Disabling the device, the typical supply shutdown current is 1

A resistor connected between SW pin and the FSW pin sets the switching frequency. The wide switching frequency range of 200 kHz to 1.0 MHz offers optimization on efficiency or size of filter components.

The SCT12A2 provides PGATE pin to control the gate of an external load disconnection P-channel MOSFET, which completely disconnects the load from the input during output shutdown condition. During start-up, the SCT12A2 gradually turns on the load disconnection switch to limit the inrush current.

The SCT12A2 device features adjustable soft-start time, cycle-by-cycle low-side FET current limit, over-voltage protection, and over-temperature protection.

The SCT12A2 uses two separate ground pins to avoid ground bouncing due to the high switching current through the N-channel power MOSFET. AGND pin sets the reference for all control functions. The source of the power MOSFET connects to PGND pin. Both grounds must be connected to the thermal pad on the PCB at the closest point.

VIN Power

The SCT12A2 is designed to operate from an input voltage supply range between 2.7 V to 20V. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is ceramic or 2 x 22uF.

VCC Power

The internal VCC LDO provides the bias power supply for internal circuitries. A ceramic capacitor of no less than 1uF is required to bypass from VCC pin to ground. During starting up, input of VCC LDO is from VIN pin. Once the output voltage at VOUT pin exceeds VIN voltage, VCC LDO switches its input to VOUT pin. This allows higher voltage headroom of VCC at lower input voltage. The maximum current capability of VCC LDO is 130mA typical. No additional components or loading are recommended on this pin.

Under Voltage Lockout UVLO

The SCT12A2 features UVLO protection for voltage rails of VIN, VCC and BOOT-SW from the converter malfunctioning and the battery over discharging. The default VIN rising threshold is 2.6V typical at startup and falling threshold is 2.4V typical at shutdown. The internal VCC LDO dropout voltage is about 100mV and the device is disabled when VCC falling trips 2.1V typical threshold. The internal charge pump from BOOT to SW powers the gate driver to high-side MOSFET Q2. The BOOT UVLO circuit monitors the capacitor voltage between BOOT pin and SW pin. When the voltage of BOOT to SW falls below a preset threshold 3V typical, high-side MOSFET Q2 turns off. As a result, the device works as a non-synchronous boost converter.

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Enable and Start-up

When applying a voltage higher than the EN high threshold (maximum 1.2V), the SCT12A2 enables all functions and starts converter operation. To disable converter operation, EN voltage needs fall below its lower threshold (minimum 0.4V). the ground. Floating EN pin automatically disables the device.

The SCT12A2 features programmable soft start to prevent inrush current during power-up. SS pin sources an internal 5 current charging an external soft-start capacitor C_{SS} when EN pin exceeds turn-on threshold. The device uses the lower voltage between the internal voltage reference 1.2V and the SS pin voltage as the reference input voltage of error amplifier and regulates the output. The soft-start completes when SS pin voltage exceeds the internal 1.2V reference. Use equation 1 to calculate the soft-start time (10% to 90%). When EN pin is pulled low to disable the device, the SS pin will be discharged to ground.

(1)

where

t_{SS} is the soft start time
V_{REF} is the internal reference voltage of 1.2V
C_{SS} is the capacitance connecting to SS pin
I_{SS} is the source current of 5uA to SS pin

Adjustable Switching Frequency

The SCT12A2 features adjustable switching frequency from 200kHz to 1.0MHz.

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I_{LIM} is the peak current limit
R_{LIM} is the resistance between ILIM pin to ground.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Load Disconnection Control

For both non-synchronous and synchronous boost converter, there is a non-fully controlled current path from converter input to output load through the diode or the high-side MOSFET body diode. During start up, once VIN is present, VOUT is moved to VIN level due to the direct path from input to output even when the device is shut down or the load is not ready. The presence of unwanted output voltage before system start up sequence could cause system to latch off or malfunction.

To address the above issues, the SCT12A2 provides a solution to insert an external P-channel MOSFET to disconnect the load from the converter output in application as shown in Figure 13. Choosing a lower R_{dson} of the disconnection P-channel MOSFET Q3 reduces impact on the efficiency. The source of Q3 needs connect to VOUT pin. Output capacitor is required at both VOUT pin and the source of P-channel MOSFET to maintain the loop stability.

In Figure 13, PGATE pin connecting to gate of Q3 has a constant sink current pulling down capability and a resistance pulling up capability. During SCT12A2 starting up, internal circuitry softly starts up of P-channel MOSFET. When gate-source voltage of external P-channel MOSFET is lower than the threshold voltage, the Q3 is turned on and the load is connected to VOUT pin. The source-gate voltage of external P-channel MOSFET is clamped up to 8V when the P-channel MOSFET is fully turned on.

When the Enable is disabled or the input voltage lower than the VIN UVLO threshold, the SCT12A2 shuts off the external P-channel MOSFET and disconnect the load

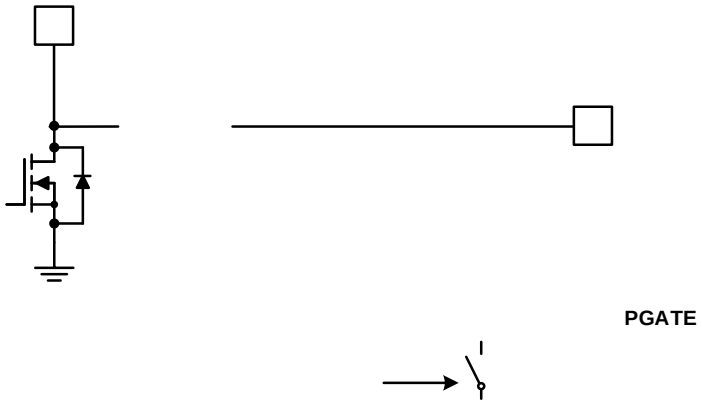

Figure 13. Load Disconnection Control

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Over Voltage Protection and Minimum On-time

The SCT12A2 features both VOUT pin over voltage pro

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user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor SMD7443552150 is used on SCT12A2 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max (mΩ)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
WE-HCI SMD 7443552150	1.5	5.3	17 / 14	10.5 x 10.2 x 4.0	WurthElektronix

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1 recommended to be placed as close as possible to the VIN pin of the SCT12A2. A ceramic capacitor of more than 1.0 internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22 or 47uF input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, three 22 ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 9 and 10 to calculate the minimum required effective capacitance, C_{OUT}.

(9)

(10)

where

V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
V_{IN_MIN} is the minimum input voltage of boost converter.
V_{OUT} is the output voltage.
I_{OUT} is the output current.
I_{Lpeak} is the peak current of the inductor.
$_{SW}$ is the converter switching frequency.
ESR is the ESR resistance of the output capacitors.

External P-channel MOSFET Selection

To minimize the power efficiency impact on the boost system, the external P-channel MOSFET with smaller R_{dson} is inserted between the converter output and load circuit to implement the load disconnection protection. The SCT12A2 provides the gate drive capability for the external P-channel MOSFET, the maximum V_{GS} of the P-channel MOSFET is clamped up to -7.1V typically if the VOUT is higher than 7.1V. Otherwise, the maximum V_{GS} follows the VOUT pin voltage in the application. As a result, the low R_{dson} and low threshold P-channel MOSFET is preferred. Table 5 shows the recommended P-channel MOSFET details.

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Table 5. Recommended External P-channel MOSFET

Part Number	R_{dson} (mΩ)	I_D (A)	Max V_{DS} (V)	Max V_{GS} (V)	Vendor
FDMC612PZ	8.4	14	-20	±12	Fairchild
CSD25404Q3	5.5	18	-20	±12	Texas Instruments

Loop Stability

An external loop compensation network comprises resister R5, ceramic capacitors C8 and C9 connected to the COMP pin

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(16)

where

f_C is the selected crossover frequency.

(17)

(18)

If the calculated value of C9 is less than 10pF, it can be left open. Designing the loop for greater than 45ὸf phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

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Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple. The placement and ground trace for C6 is critical for the performance of SW ringing voltage. Place capacitor C6 as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin.

The layout should also be done with well consideration of the thermal. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias (8mil) underneath the thermal pad. The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias. Since thermal pad is electrical power ground of the device, improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias

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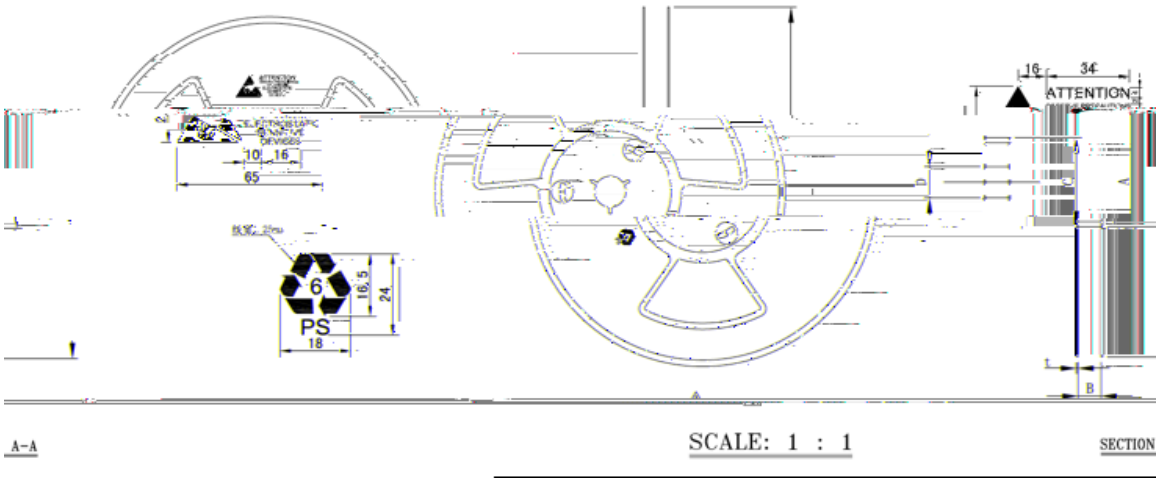
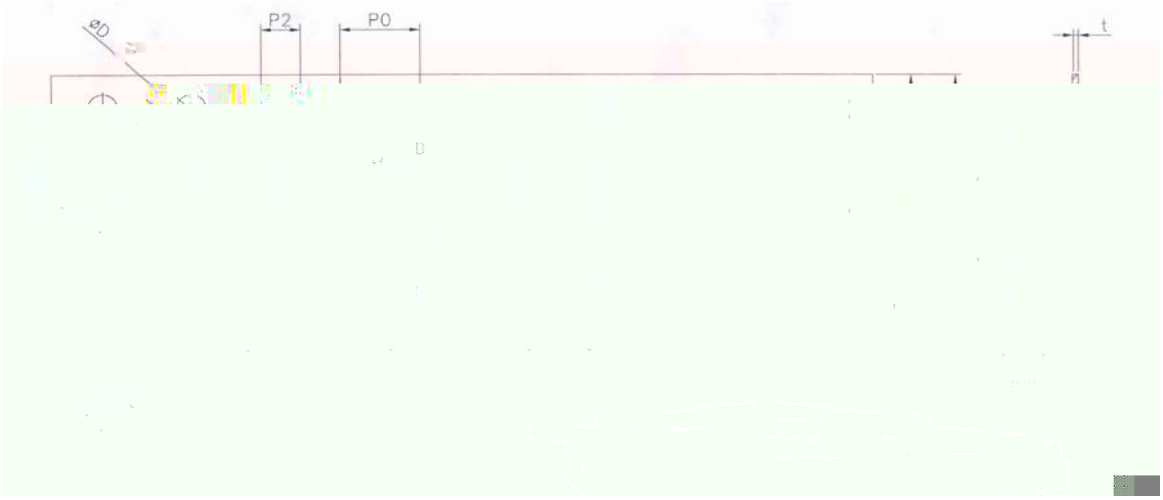
TAPE AND REEL INFORMATION



REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3



TYPE DIMENSIONS

W (mm)	A0 (mm)	B0 (mm)	K0 (mm)	t (mm)	P (mm)
12±0.30	3.80±0.10	4.80±0.10	1.18±0.10	0.30±0.05	8±0.10

E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)
1.75±0.10	5.50±0.10	2.00±0.10	1.55±0.10	1.50MIN	4.00±0.10	40.0±0.20

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RELATED PARTS

PART NUMBERS	DESCRIPTION	COMMENTS
SCT12A3	15-A Fully-integrated Synchronous Boost Converter	Vin=2.7V-20V, 15A switch peak EMCCg7/Lang (Er6(nt

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