5 to 60V Three-Phase Brushless DC Motor Pre-Driver

FEATURES

- Wide Operating Voltage: 5V to 60V
- Charge Pump Gate Drive Supply
- 100% Duty Operation with Trickle Charge Circuit
- 1A Maximum Peak Source Current
- 2A Maximum Peak Sink Current
- 3.3V and 5V Logic Compatible
- Low-Power Sleep Mode
- Adjustable Dead-Time
- Fault Indication and Two Level (3-State) MCU Protection

REVISION HISTORY

Revision 0.8: Customer Sample.

Revision 0.81: Update DEVICE ORDER INFORMATION.

DEVICE ORDER INFORMATION

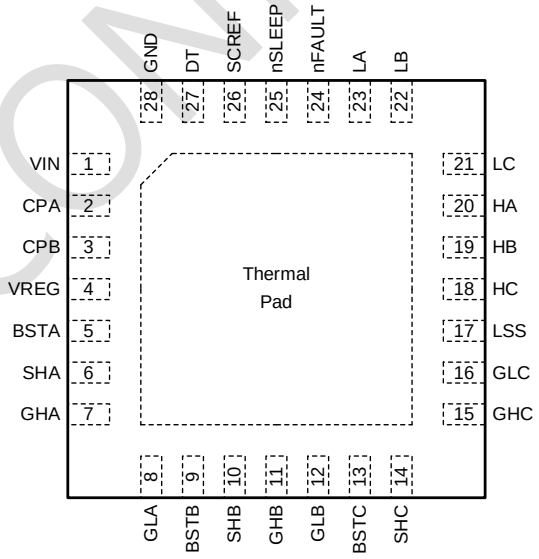
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT55611QZAR	Tape & Reel	3000	5611	28	QFN-28L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	65	V
CPA	-0.3	13	V
CPB	-0.3	6	V
VREG	-0.3	13	V
BSTA - SHA, BSTB - SHB, BSTC - SHC	-0.3	13	V
GHA - SHA, GHB - SHB, GHC - SHC	-0.3	13	V
SHA, SHB, SHC	-0.3	65	V
GLA, GLB, GLC	-0.3	13	V
LSS	-0.3	1	V
HA, HB, HC, LA, LB, LC, DT, SCREF, nSLEEP, nFAULT,	-0.3	6	V
Operation junction temperature T_J (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 28-Lead QFN 4mm×4mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes thermal shutdown protection to protect the device during overload conditions. Junction temperature will exceed 175°C when thermal shutdown protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	PIN	PIN FUNCTION
VIN	1	Input supply voltage. Connect a bypass capacitor close to the pin.
CPA	2	Charge pump switching node. Connect a ceramic capacitor between CPA and CPB.
CPB	3	
VREG	4	Gate driver supply output. Connect a ceramic capacitor to ground.
BSTA	5	Phase A bootstrap pin. Connect a ceramic capacitor between BSTA and SHA.
SHA	6	Phase A high-side source pin. Connect to the source of high-side FET.
GHA	7	Phase A high-side gate driver output. Connect to the gate of high-side FET.
GLA	8	Phase A low-side gate driver output. Connect to the gate of low-side FET.
BSTB	9	Phase B bootstrap pin. Connect a ceramic capacitor between BSTB and SHB.
SHB	10	Phase B high-side source pin. Connect to the source of high-side FET.
GHB	11	Phase B high-side gate driver output. Connect to the gate of high-side FET.
GLB	12	Phase B low-side gate driver output. Connect to the gate of low-side FET.
BSTC	13	Phase C bootstrap pin. Connect a ceramic capacitor between BSTC and SHC.
SHC	14	Phase C high-side source pin. Connect to the source of high-side FET.
GHC	15	Phase C high-side gate driver output. Connect to the gate of high-side FET.
GLC	16	Phase C low-side gate driver output. Connect to the gate of low-side FET.
LSS	17	Low-side source pin. Connect to the sources of phase A/B/C low side FET.
HC	18	Phase C high-side drive signal input pin. Internal pulldown.
HB	19	Phase B high-side drive signal input pin. Internal pulldown.
HA	20	Phase A high-side drive signal input pin. Internal pulldown.
LC	21	Phase C low-side drive signal input pin. Internal pulldown.
LB	22	Phase B low-side drive signal input pin. Internal pulldown.
LA	23	Phase A low-side drive signal input pin. Internal pulldown.
nFAULT	24	Fault indication output pin. Open-drain output and pulled low when in a fault condition. Connect an external pull-up resistor to an external supply.
nSLEEP	25	Sleep mode input pin. Logic low to enter low-power sleep mode and high to exit. Internal pulldown.
SCREF	26	Short circuit protection reference input pin.
DT	27	Dead-time setting pin. Connect a resistor to ground to set the dead-time.
GND	28	Ground.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	5	60	V
V_{SCREF}	SCREF voltage	0.125	2.4	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-1.5	+1.5	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-28L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	39.9	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	44.85	
$R_{\theta JC\ (bot)}$	Junction to case (bottom) thermal resistance(1)	6.6	
$R_{\theta JB}$	Junction to board thermal resistance(1)	18.15	
$R_{\psi JT}$	Junction-to-top characterization parameter	5.05	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT55611 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT55611. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

Typical values correspond to V_{IN} = 24V, T_A = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Input Supply Voltage		5		60	V
I_Q	Quiescent Current	nSLEEP = 1, gate not switching		1	2	mA

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
nFAULT (Open-Drain Output)						
V_{OL}	Output low voltage	I_O=5mA			0.5	V
I_{OH}	Output high leakage current	V_O=3.3V			1	uA
Protection Circuits						
V_{IN_RISE}	VIN UVLO Rising Threshold			4.2	4.5	V
V_{IN_HYS}	VIN UVLO Hysteresis			200		mV
V_{REG_RISE}	VREG UVLO Rising Threshold			7.6		V
V_{REG_HYS}	VREG UVLO Hysteresis			1.6		V
V_{SC}(1)	Short-Circuit Threshold Accuracy (MOSFET V_{DS})	V_{SCREF}=1V, T_J=25°C	0.8	1	1.2	V
		V_{SCREF}=2.4V, T_J=25°C	2.18	2.4	2.62	V
t_{OC}	OCP Deglitch Time			3		us
t_{SLEEP}	SLEEP Wakeup Time	VREG cap=10uF		250		us
$V_{LSS-OCP}$	LSS OCP threshold		0.4	0.5	0.6	V
T_{TSD}	Thermal Shutdown			175		°C
V_{BSTUV}	BSTx-SWx Falling Threshold			4.3		V
Gate Driver						
V_{FBOOT}	Bootstrap Diode Forward Voltage	I_D=10mA		1		V
V_{REG}	VREG Output Voltage	V_{IN}=6~60V	10.5	11.3	12	V
		V_{IN}=5~6V	9			V
I_{OSO}	Maximum source current			1		A
I_{OSI}	Maximum sink current			2		A
R_{UP}	Gate drive pull-up resistance	V_{DS}=1V		6		Ω
R_{HS_DN}	HS gate drive pull-down resistance	V_{DS}=1V	0.2		3	Ω
R_{LS_DN}	LS gate drive pull-down resistance	V_{DS}=1V	1		2.5	Ω
f_{CP}	Charge pump frequency			110		kHz

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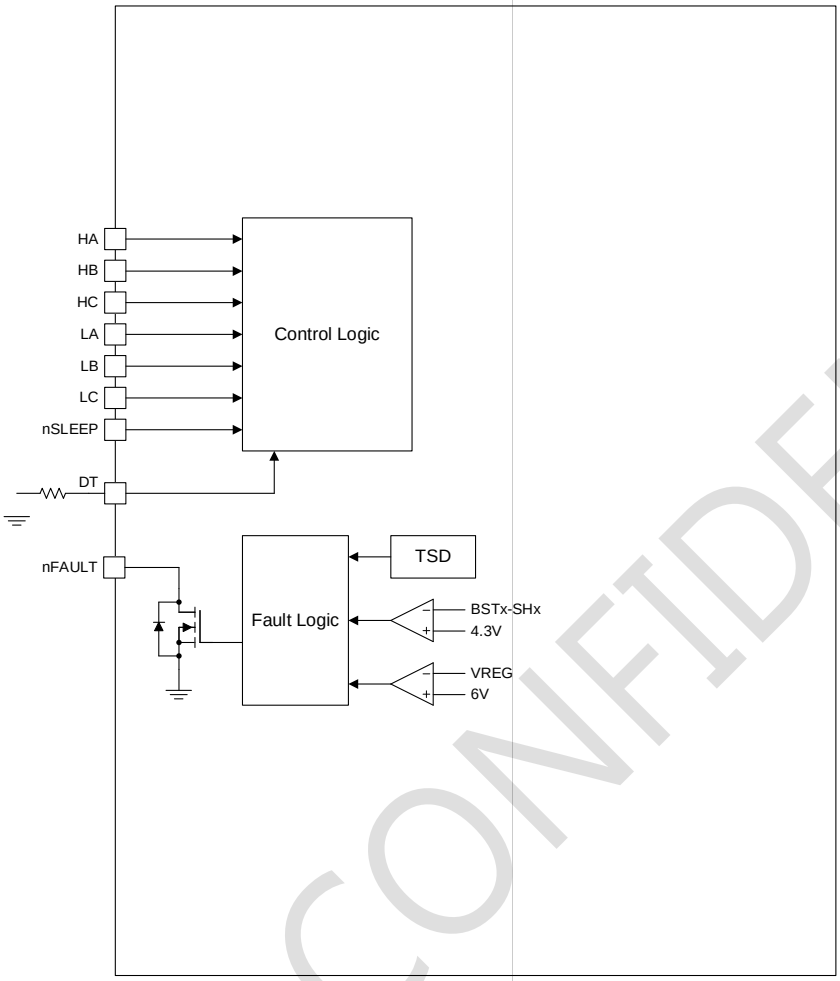
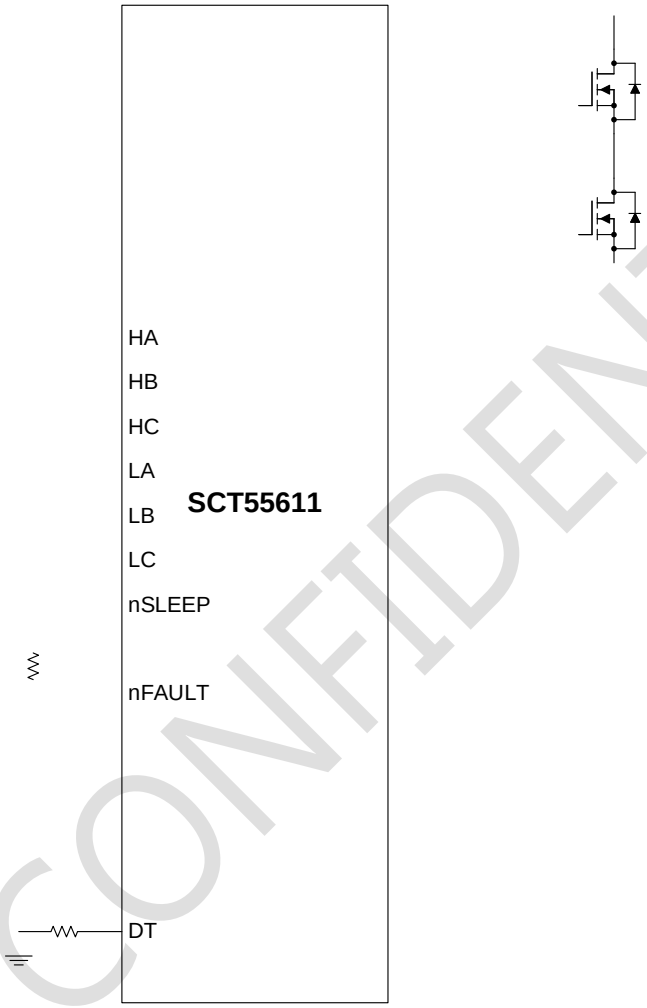
FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

Typical Application



Driver Power Dissipation

Generally, the power dissipation in the SCT55611 depends on the driver-stage loss and V_{REG} regulation loss.

The power loss of a single gate driver can be estimated by Equation (2):

(2)

where

- Q_g is the total gate charge of the power device
- f_{SW} is the switching frequency
- V_{REG} is the gate drive voltage

If the gate resistor R_G applied between the driver output and gate of power device to slow down the switching transition, the power loss of a single gate driver can be estimated by Equation (3):

(3)

where

- R_{UP} is the gate driver pull-up resistance
- R_{DN} is the gate driver pull-down resistance
- R_G is the external resistance between the driver output and gate of power device

For a typical three-phase BLDC motor control, always only one of the three half-bridges are switching at f_{SW} during the whole rotation cycle. In this case, the total driver-stage power dissipation can be estimated by one half-bridge, namely a high-side gate driver and a low-side gate driver.

The gate drive voltage V_{REG} is generated from VIN through either a charge pump when VIN is low or a LDO when VIN is high. The power loss of V_{REG} regulation can be estimated referring to Table 3:

Table 3. V_{REG} Regulation Loss

Input Range	Mode	Power Loss Equation
VIN < 16V	Charge Pump	–
VIN > 16V	LDO	–

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (4):

–

θJA (4)

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table

The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

Application Waveforms

V_{IN} = 24V, V_{SCREF} = 0.5V, f_{PWM} = 20kHz, T_A = 25°C, unless otherwise noted.

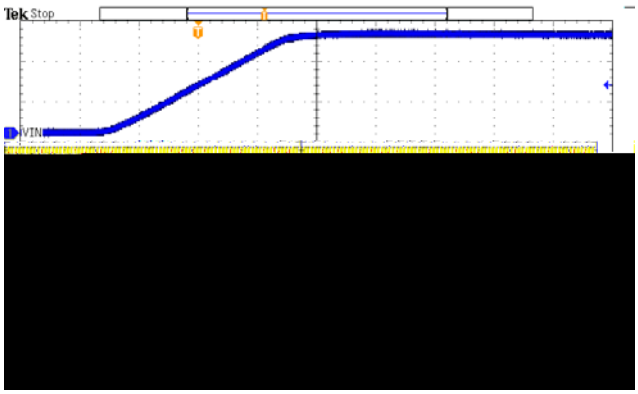


Figure 9. Power Ramp Up

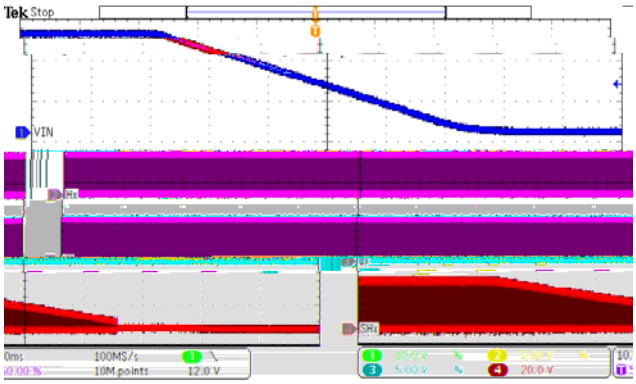


Figure 10. Power Ramp Down

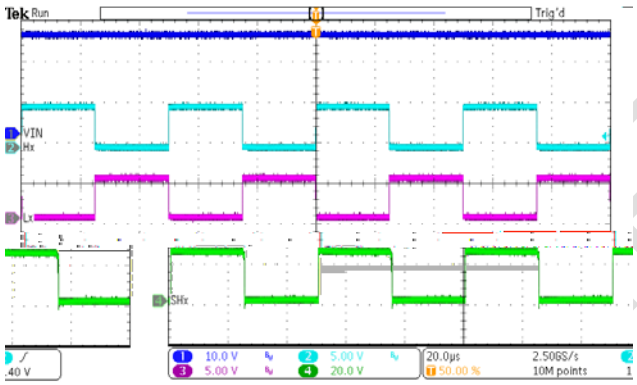


Figure 11. Steady State

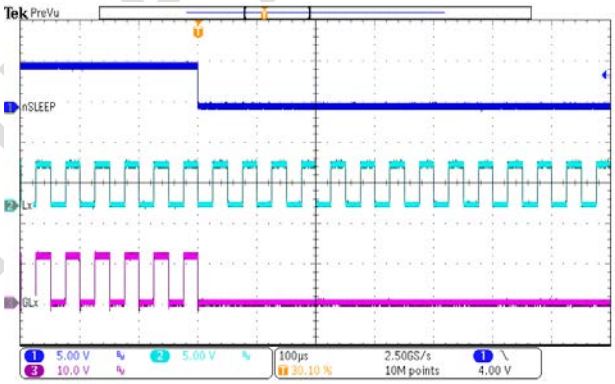


Figure 12. Sleep Mode Entry

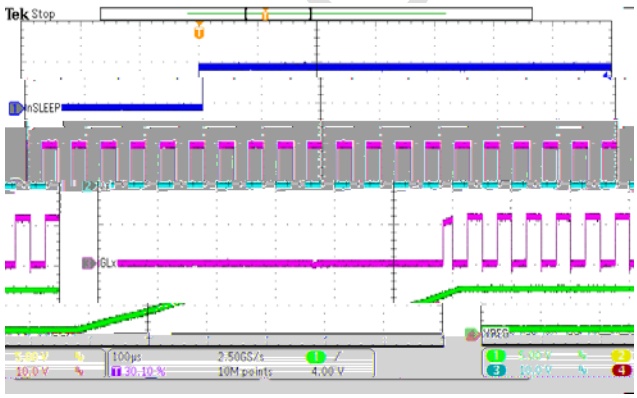


Figure 13. Sleep Mode Recovery

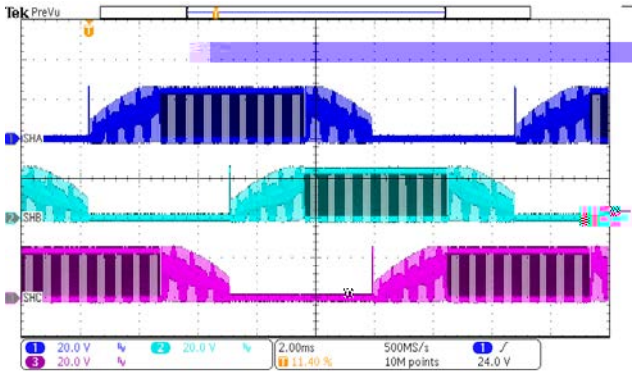


Figure 14. 3-Phase BLDC Motor Operation

Layout Guideline

The SCT55611 provides high output driving current and features very short rising and falling time at the gate of power device. The high di/dt might cause driver output unexpected ringing when the driver output loop is not designed well. The system could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. For better performance, follow the layout guidelines as shown below.

1. Put the SCT55611 as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate.
2. Place the power supply decoupling capacitors as close as possible to the VIN pin. Low-ESR ceramic capacitors of type X5R or X7R are recommended.
3. Place the VREG capacitor close to VREG pin.
4. Place the charge pump capacitor close to CPA and CPB pins with minimized loop.
5. Place the bootstrap capacitors close to BSTx and SHx pins with minimized loop.
6. For the low-side sense resistor for over current protection, it is recommended to use a wide-package resistor or paralleled resistors to minimize the parasitic inductance introduced between the LSS pin and ground.
7. At least one ground plane is recommended to provide noise shielding and thermal dissipation. The device thermal pad should be soldered to the top-layer ground plane with multiply vias connected to the bottom-layer ground plane to achieve better thermal performance.

PACKAGE INFORMATION