-		
VDD	8	Output voltage of the Buck converter. Connect 22uF capacitor from this pin to GND pin. VDD is also the input power supply for gate driver of power stage, the 3.3V LDO and the 2.5V voltage reference.
V3P3	9	3.3V LDO output. Connect 1uF capacitor to ground.
BST2	10	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	11	Switching node of the half-bridge FETs Q3 and Q4.
SW1	12	Switching node of the half-bridge FETs Q1 and Q2.
BST1	13	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
VREF	14	Output of the 2.5V LDO. Connect a 1uF capacitor to ground.
ISNS	15	Current detection output. The voltage of the pin is proportional to the input current.
AGND	16	Analog ground of the IC
PWM2	17	



# **SCT63240**

board (PCB) on which the SCT63240 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63240. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R.

## C KI C I K I K

V<sub>IN</sub>=V<sub>PVIN1</sub>=V<sub>PVIN2</sub>=12V, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supp	lies and UVLO					
V <sub>IN</sub>	Operating input voltage		4.2		20	V
P <sub>VIN</sub>	Operating input voltage		1		17	V
V <sub>IN_UVLO</sub>	V <sub>IN</sub> UVLO Threshold Hysteresis	V <sub>IN</sub> rising		3.6 400		V mV
V <sub>DD_UVLO</sub>	V <sub>DD</sub> UVLO Threshold Hysteresis	V <sub>DD</sub> rising		3.8 440		V mV
I <sub>SHDN</sub>	Shutdown current from VIN pin	EN=0V, VIN=12V		1	3	Α
Ishdn_pvin	Shutdown current from PVIN1,PVIN2	EN=0V, PVIN=12V		1	3	uA
I <sub>SHDN_VDD</sub>	Shutdown current from VDD	EN=0V, VDD=5.5V		18	35	uA
IVINQ	Quiescent current from VIN pin	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		210		uA
IPVINQ	Quiescent current from PVIN1, PVIN2	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		50		uA
lα	Quiescent current from VDD pin	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		270		uA
ENABLE IN	IPUTS and PWM logic					
V <sub>EN_H</sub>	Enable high threshold			1.18		V
V <sub>EN_L</sub>	Enable low threshold			1.1		V
VIH	PWM1, PWM2 Logic level high	V3P3=3.3V, VDD=5V	2.65			V
VIL	PWM1, PWM2 Logic level low	V3P3=3.3V, VDD=5V			0.55	V
V <sub>TS</sub>	PWM1, PWM2 Tri-state voltage		1.2		2	V
Power Stag	re					
R <sub>DSON_Q1</sub>	High-side MOSFETQ1 on-resistance	V <sub>BST1</sub> -V <sub>SW1</sub> =5V		13		m
RDSON_Q2	Low-side MOSFETQ2 on-resistance	VDD=5V		13		m
R <sub>DSON_Q3</sub>	High-side MOSFETQ3 on-resistance	V <sub>BST2</sub> -V <sub>SW2</sub> =5V		13		m
RDSON_Q4	Low-side MOSFETQ4 on-resistance	VDD=5V		13		m
I <sub>LIM</sub>	How-side current limit threshold			12.5		Α
Buck conv	erter		-			•
F <sub>SW</sub>	Switching frequency		540	600	660	KHz
V <sub>DD</sub>	Output voltage		4.925	5	5.075	V
I <sub>LIM_HS</sub>	High-side power MOSFET peak current limit threshold			1.5		А

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R <sub>DSON_L</sub>	Low side FET on-resistance			200		
T <sub>SS</sub>	Internal soft-start time			2		ms
3.3V LDO						
V <sub>3P3</sub>	Output voltage	Cout=1uF, VDD=5V	3.267	3.3	3.333	V
I <sub>3P3</sub>	Output current Capability			200		mA
Isc <sub>1</sub>	Short current			50		mA
2.5V REFFI	ERENCE OUTPUT					
V <sub>2P5</sub>	Output voltage reference	Cout=1uF, VDD=5V	2.475	2.5	2.525	V
I <sub>3P3</sub>	Output current Capability			100		mA
I <sub>SC2</sub>	Short current			40		mA
Current Se	nse					
V <sub>ISNS0</sub>	Voltage with no input current	I <sub>PGND</sub> =0A ,Tj=25 PWM1=PWM2=0V	0.585	0.6	0.615	V
R <sub>ISNS</sub>	Input current to output voltage gain	VISNS=VISNS0+IPGND*RISNS	0.98	1	1.02	V/A
V <sub>ISNS1</sub>	Voltage with 0.6A input current	I <sub>PVIN</sub> =0.6A, Tj=25	1.176	1.2	1.224	V
V <sub>ISNS2</sub>	Voltage with 1A input current	I <sub>PVIN</sub> =1A, Tj=25	1.568	1.6	1.632	V
Protection						
T <sub>SD</sub>	Thermal shutdown threshold	T <sub>J</sub> rising		155		°C
	Hysteresis	MINISTER Actions Student		35		°C



KPG C I K I K

Figure 2. Transfer Efficiency with 5W RX@ Vout=5V

Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

Figure 4.



# ②LE KFE C CF B I D

PWM1

**」**┡

Figure 8. Functional Block Diagram

### FG I KFE

#### Overview

The SCT63240 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V buck converter as power supply for external transmitter controller and internal 5V power supply to increase system efficiency, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU and a 2.5V reference voltage.

The SCT63240 has four power input pins. VIN is connected to the power FETs of buck converter. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer. VDD is the output feedback pin of the 5V output buck converter and at the mean while as the power supply for internal two LDOs and full bridge MOSFET's gate driver.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.2V typically. The maximum operating voltage for PVIN is up to 20V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63240 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The buck converter and full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63240 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for buck converter and 4-MOSFETs full bridge, current limit and current fold back at hard short for two LDOs and whole chip thermal shutdown protection.

### **Enable and Start up Sequence**

When the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.18V, the buck converter and two LDOs enable at once. And the device disables when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.1V. VDD ramp up after buck converter works, and also the V3V and VREF output do. Once VDD rise up to 3.8V and V3V is higher than 3V, 4-MOSFETs full bridge allows PWM signal to control for switching. PWM input cannot control full bridge of MOSFETs if VDD drop to 3.36V or V3V drop to 2.7V.

An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin is floating to simply the system design. If an application requires a higher system under voltage lockout threshold, two external resistors divider(R1 and R2) in Figure 9 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

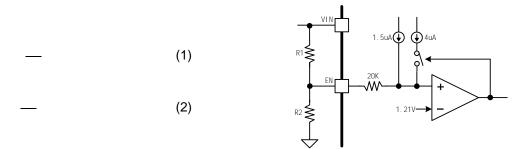


Figure 9. System UVLO by enable divider



**5V Output Buck Converter** 



#### **Full Bridge Over Current Protection**

The SCT63240 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 12.5A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

### **Current Sense**

The SCT63240 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with ±2% accuracy and reports a proportional voltage directly to the ISNS pin. This voltage information on ISNS pin can be send to specialized controller or general MCU for Foreign Object Detection FOD and current demodulation.

When the full bridge of MOSFETs does not work, no current flows to PGND. The DC bias voltage on ISNS pin is 600mV. This DC bias helps set up a suitable voltage bias for the following analog to digital converter in MCU or amplifier for current demodulation. The average input current to voltage conversion gain on ISNS is 1V/A. The equation 3 represent the corresponding relation for the output voltage on ISNS pin and average current to PGND from full bridge.

(3)

#### **3.3V LDO**

The SCT63240 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 200mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

### **VREF Voltage Reference Output**

The SCT63240 also has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 2.5V voltage on VREF pin. The accuracy of the VREF voltage is ±1% and output current capability is 100mA. This voltage regulator can be used as the supply voltage or a reference voltage to external IC and circuit.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VREF pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

#### **Thermal Shutdown**

The SCT63240 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155C, the thermal sensing circuit stops Buck converter, two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120C, then the device restarts.



# GGC KFE E2FID KFE

# **Typical Application**

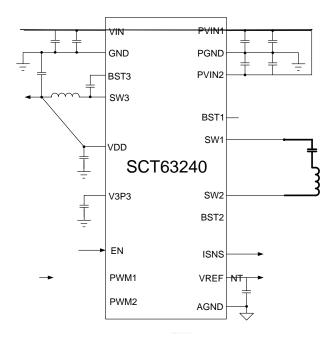


Figure 10. Same Input to VIN and PVIN

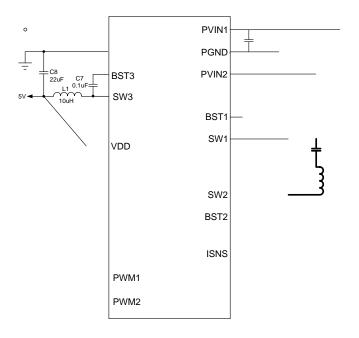


Figure 11. Separate Input to VIN and PVIN



## **Application Waveforms**

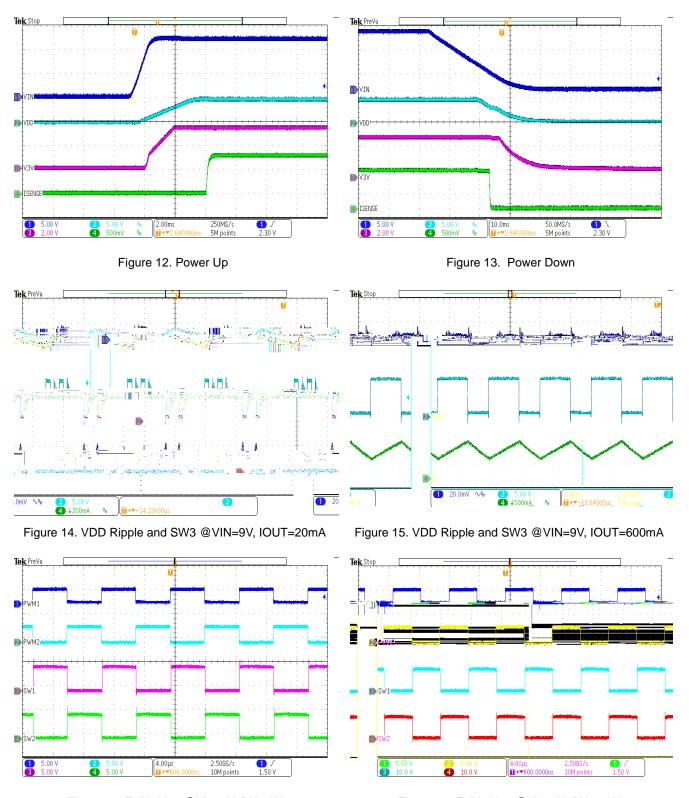


Figure 16. Full bridge @Vin=5V, RX=5W

Figure 17. Full bridge @Vin=9V, RX=10W



## **Layout Guideline**

Proper PCB layout is a critical for SCT63240

currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

- 1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
- 2. PGND connect to bottom layer by via between capacitors.
- 3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
- 4. Buck converter output capacitor's ground should connect to GND directly to minimize the power loop.
- 5. VDD pin can connect to the DC/DC's output capacitor from bottom layer, connect to the point behind the capacitor while not connect to inductor.
- 6. Bypass capacitor for VDD place next to VDD pin.
- 7. Bypass capacitor for V3P3 place next to V3P3 pin.
- 8. Bypass capacitor for VREF place next to VREF pin.
- 9. AGND pin connect to common ground by Kelvin connection.

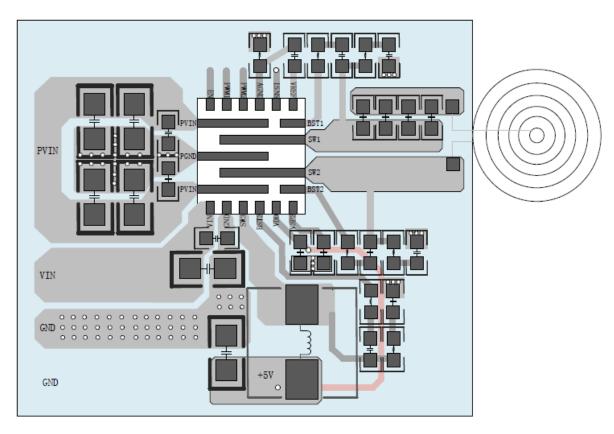
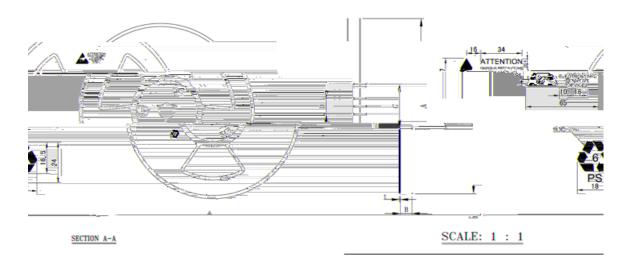


Figure 24. PCB Layout Example

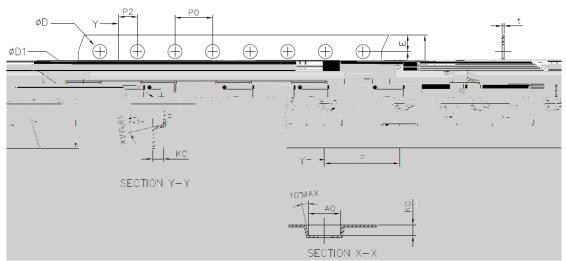


# KG EI CE2FID KFE



### REEL DIMENSIONS

Reel Width	Α	В	С	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3



TAPE DIMENSIONS

W		A0	B0	K0	t	Р
(mm)		(mm)	(mm)	(mm)	(mm)	(mm)
		3.40±0.10	4.40±0.10	1.14±0.10	0.25±0.02	8±0.10
Е	F	P2	D	D1	P0	10P0
(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)

