- Wide supply rail from 8V-24V
- Drives Both High-side and Low-side N-Channel MOSFET
- 4A Peak Output Source and Sink Current
- Bootstrap Supply Voltage Range up to 120V
- Integrated Bootstrap Diode
- TTL Compatible Input, -10V Input Capability
- Quiescent Current 252uA
- 45ns Propagation Delay Times
- 2ns Delay Matching
- 7ns Rise and 4.5ns Fall Time with 1000pF Load
- 15ns Input Deglitching Time
- 40ns Minimum Pulse Width
- Supply Rail Under-Voltage Lockout (UVLO)
- Operation from -40°C~150°C
- Available in SOP-8L, ESOP-8L, DFN-9L 3mm x 3mm, DFN-10L 3mm x 3mm and DFN-8L 4mm x 4mm Package

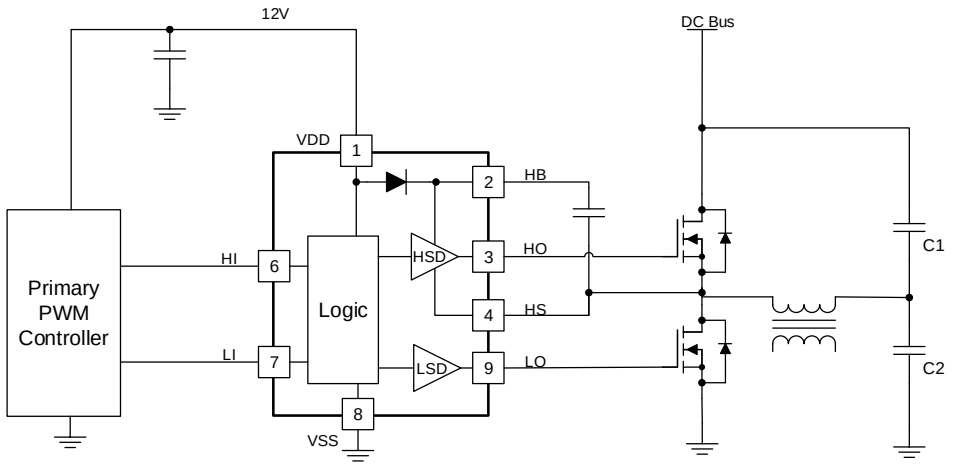
The SCT52A40 is a wide supply, high frequency gate drivers including both high side and low side drivers, which are used in half-bridge, full-bridge, and buck converter to drive the discrete N-Type MOSFETs. 4A Peak Source and Sink current capability increase the power converter power efficiency.

The SCT52A40 features wide input hysteresis that is compatible for TTL low voltage logic. The SCT52A40 has the capability to handle negative input down to -10V, which increases the input noise immunity. The ability to withstand maximum of -18V on HS pin largely extend the SCT52A40 application flexibility to handle the switching node noise.

The 40ns minimum pulse width enables the SCT52A40 suitable for high frequency power converter application.

The SCT52A40 is available in DFN-9L 3mm x 3mm, DFN-8L 4mm x 4mm, ESOP-8L and SOP-8L package.

- Battery Powered Hand Tool
- Solid-State Motor Drives
- Half-Bridge and Full-Bridge Power Converter
- Two Switch Forward Power Converters
- Active-Clamp Forward Converters



NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Add SCT52A40DRA

Revision 1.2: Add HS pulse voltage spec in ABS max rating table

Revision 1.3: Add limit values for T_{MON} and T_{MOFF} in ELECTRICAL CHARACTERISTICS

Revision 1.4: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52A40DRAR	Tape & Reel	5000	2A40	10	DFN-10L
SCT52A40DSAR	Tape & Reel	5000	2A40	9	DFN-9L
SCT52A40DTCR	Tape & Reel	5000	2A40	8	DFN-8L
SCT52A40STER	Tape & Reel	4000	2A40	8	ESOP-8L
SCT52A40STDR	Tape & Reel	4000	2A40	8	SOP-8L

Over operating free-air temperature unless otherwise noted(1)

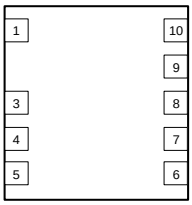
DESCRIPTION	MIN	MAX	UNIT
VDD	-0.3	26	V
HI, LI	-10	26	V
LO (DC)	-0.3	V_{DD} + 0.3	V
LO (Pulse < 100ns) (3)	-2	V_{DD} + 0.3	V
HB	-0.3	120	V
HB-HS	-0.3	26	V
HO (DC)	V_{HS} - 0.3	V_{HB} + 0.3	V
HO (Pulse < 100ns) (3)	V_{HS} - 2	V_{HB} + 0.3	V
HS (DC)	-1	120	V
HS (Pulse < 300ns) (3)	-3	120	V
HS (Pulse < 100ns) (3)	-18	120	V
Operating junction temperature TJ (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

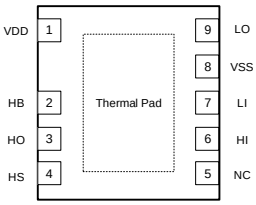
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

(3) Values are verified by characterization and are not production tested.

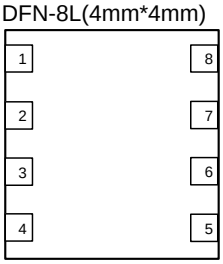
Top View
DFN-10L(3mm*3mm)



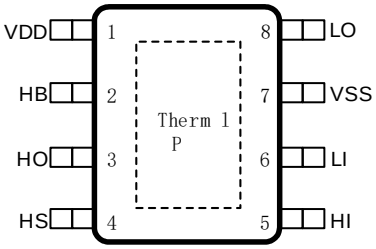
Top View
DFN-9L(3mm*3mm)



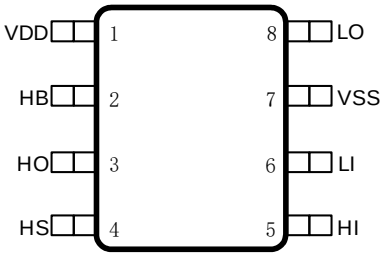
Top View
DFN-8L(4mm*4mm)



Top View
ESOP-8L



Top View
SOP-8L



NAME	DFN-10L	DFN-9L	DFN-8L	ESOP-8L	SOP-8L	PIN FUNCTION
	NO.	NO.	NO.	NO.	NO.	

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	8	24	V
$V_{HI,LI}$	Driver input voltage range	-10	24	V
V_{HS}	Voltage on HS	-1	120	V
	Slew rate on HS		50	V/ns
V_{HB}	Voltage on HB	V_{HS}+8	120	V
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	DFN-10L 3x3mm	DFN-9L 3x3mm	DFN-8L 4x4mm	ESOP-8L	SOP-8L	UNIT
R	Junction to ambient thermal resistance (1)	43.7	43.7	36.2	40.5	106.5	°C/W
R	Junction to case thermal resistance (1)	49.9	49.9	41.6	49	52.9	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT52A40 is mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT52A40. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Supply Currents						
I_{DD}	VDD quiescent current	VHI=VLI=0		252		uA
I_{VDDO}	VDD operating current	Fsw=500kHz, CLoad=0nF		2.27		mA
I_{HB}	HB quiescent current	VHI=VLI=0		168		uA
I_{HBO}	HB operating current	Fsw=500kHz, CLoad=0nF		2		mA
I_{HBS}	HB to VSS quiescent current	VHS=VHB=110V			1	uA
I_{HBSO}	HB to VSS operating current	Fsw=500kHz, CLoad=0nF		1.1		mA
INPUTS						
$V_{HI, LI}$	Input logic high threshold			2.1	2.4	V
	Input logic low threshold		0.8	1		V
V_{HI, LI_Hys}	Hysteresis			1.1		V
	Input pull down resistance			200		
UNDERVOLTAGE PROTECTION(UVLO)						
V_{DDR}	VDD rising threshold			7.18		V
V_{DDHYS}	VDD threshold hysteresis			0.63		V
V_{HBR}	HB rising threshold			6.7		V
V_{HBHYS}	HB threshold hysteresis			0.43		V
LO GATE DRIVER						
V_{LOH}	Output high voltage	I_{OUT}= - 10mA, $V_{LOH}=V_{DD}-V_{LO}$			10	mV
V_{LOL}	Output low voltage	I_{OUT}= 10mA			10	mV
$I_{SINK/SRC}$	Output sink/source peak current	C_{Load}=10nF		4		A
R_{LOH}	Output pull high resistance	I_{OUT}= - 10mA		1		
R_{LOL}	Output pull low resistance	I_{OUT}= 10mA		0.7		
HO GATE DRIVER						
V_{HOH}	Output high voltage	I_{OUT}= - 10mA, $V_{HOH}=V_{HB}-V_{HO}$			10	mV
V_{HOL}	Output low voltage	I_{OUT}= 10mA			10	mV
$I_{SINK/SRC}$	Output sink/source peak current	C_{Load}=10nF		4		A
R_{HOH}	Output pull high resistance	I_{OUT}= - 10mA		1		
R_{HOL}	Output pull low resistance	I_{OUT}= 10mA		0.7		
BOOTSTRAPE DIODE						
VFL	Low current forward voltage	IVDD - HB=100uA		0.64		V
VFH	High current forward voltage	IVDD HB=100mA		0.88		V
RD	Dynamic resistance			0.7		Ω
OUTPUT RISE AND FALL TIME						
T_{R_LO}	Low side driver output rising time	C_{Load}=1nF		7		ns
T_{F_LO}	Low side driver output falling time	C_{Load}=1nF		4.5		ns
T_{R_HO}	High side driver output rising time	C_{Load}=1nF		7		ns
T_{F_HO}	High side driver output falling time	C_{Load}=1nF		4.5		ns
T_{R_LO}	Low side driver output rising time	C_{Load}=100nF		0.4		us

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

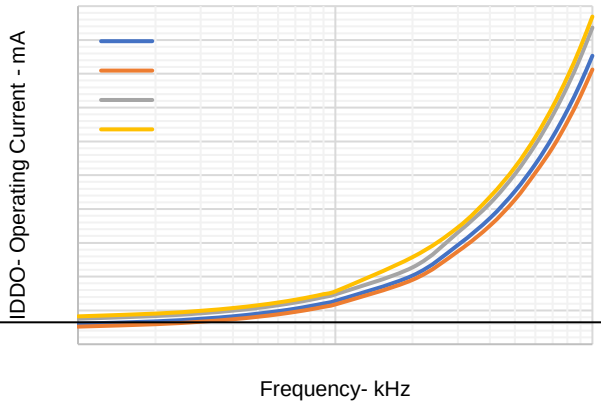


Figure 2. IDD Operating Current vs Frequency

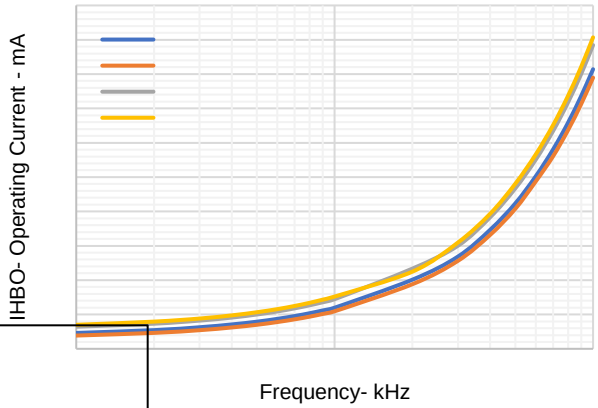


Figure 3. Boot Voltage Operating Current vs Frequency

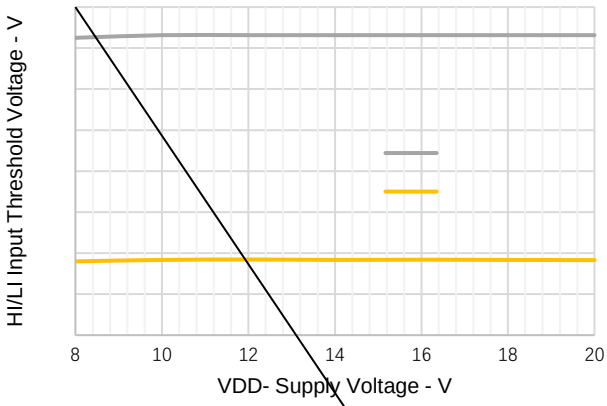


Figure 4. Input Threshold vs Supply Voltage

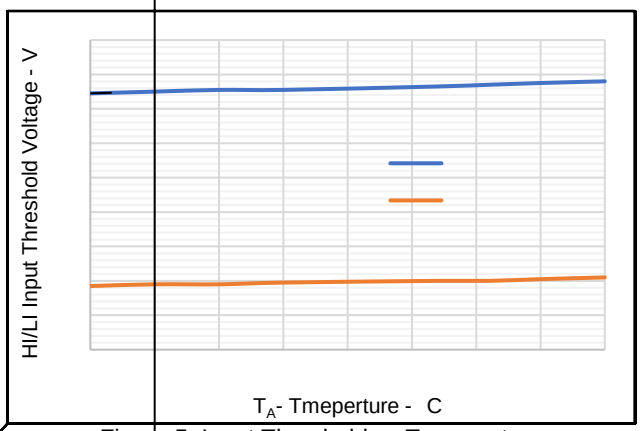


Figure 5. Input Threshold vs Temperature

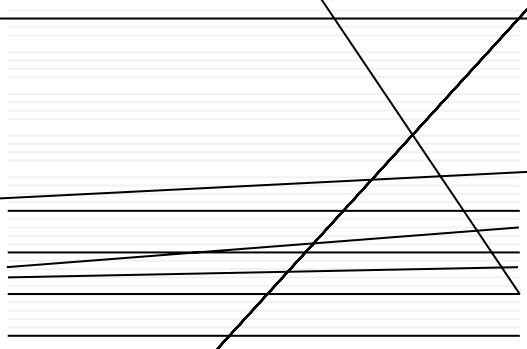


Figure 6. Output pull high resistance vs Temp

Figure 7. Output pull low resistance vs Temp

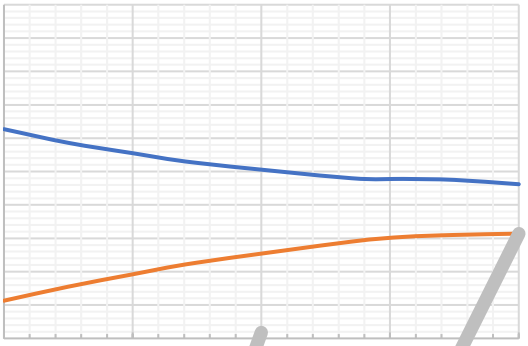


Figure 8. UVLO Threshold vs Temperature

Figure 9. UVLO Threshold Hysteresis vs Temperature

Figure 10. Propagation Delays vs Temperature

Figure 11. Propagation Delay vs Supply Voltage

Figure 12. Delay Matching vs Temperature

Figure 13. Diode Current vs Diode Voltage

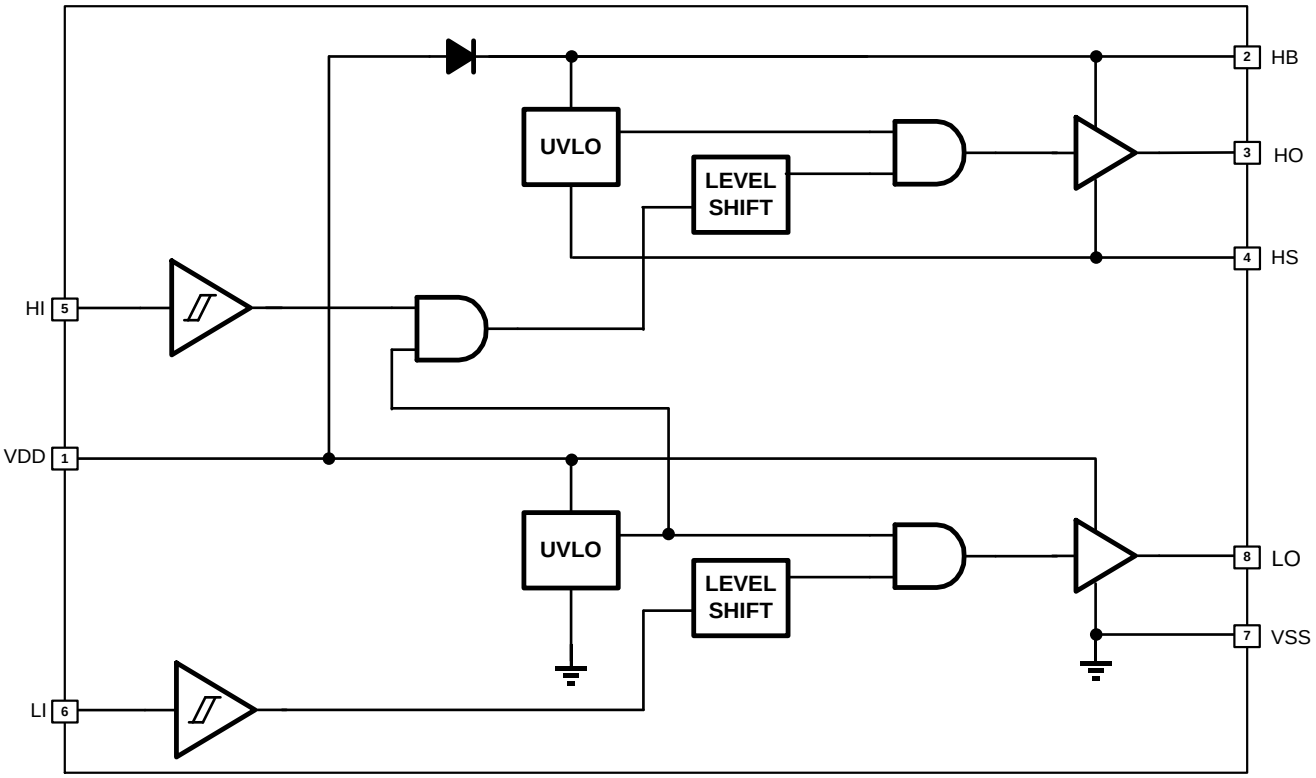


Figure 14. Functional Block Diagram

Overview

The SCT52A40 is high-side and low-side drivers. The high-side and low-side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the SCT52A40. The Input of SCT52A40 is the TTL logic compatible version. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to VSS which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

Table 1: the SCT52A40 Device Logic.

Typical Application

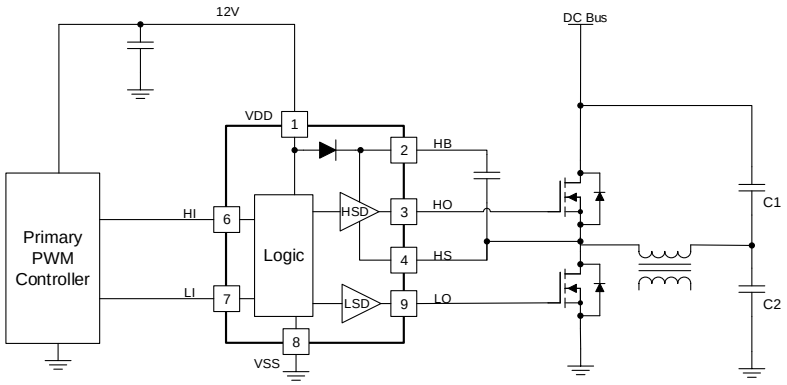


Figure 15. Dual Channel Driver Typical Application (DFN-9)

Driver Power Dissipation

Generally, the power dissipated in the SCT52A40 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52A40 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52A40 is:

$$= \quad ^2 \qquad (1)$$

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52A40 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

$$= \qquad (2)$$

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

$$= \frac{1}{2} \qquad \frac{\qquad}{+} + \frac{\qquad}{+} \qquad (3)$$

Where

- R_{OH} is the equivalent pull up resistance of SCT52A40
- R_{OL} is the pull down resistance of SCT52A40
- R_G is the gate resistance between driver output and gate of power device.

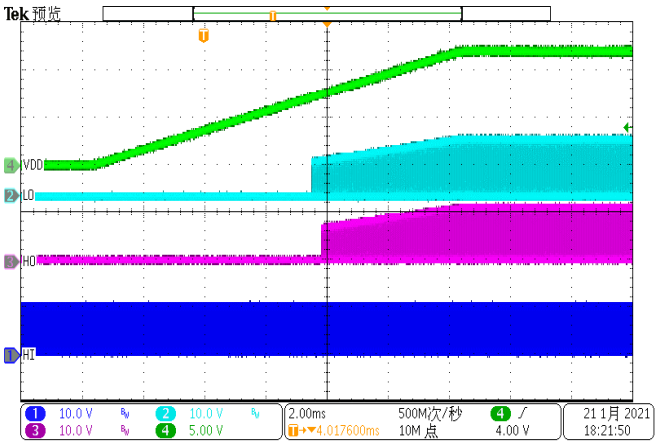


Figure 16. Power Up

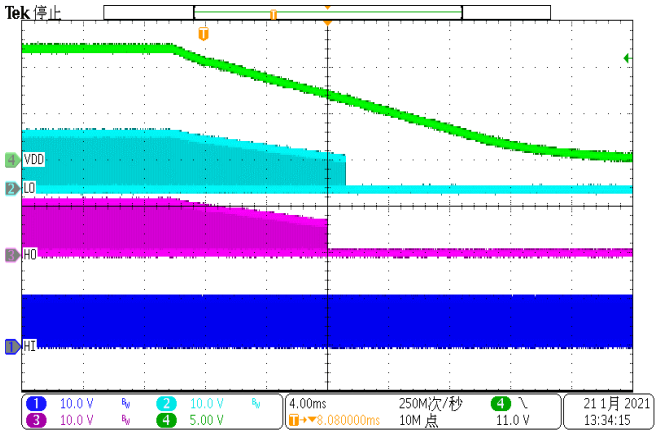


Figure 17. Power Down

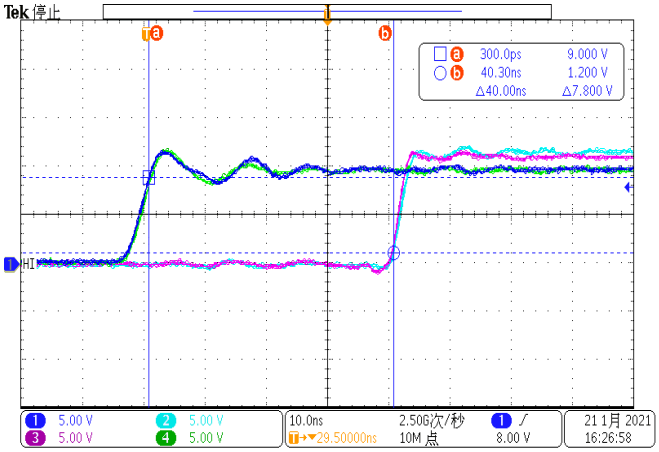


Figure 18. LO HO Rising Edge Propagation Delay, C_L=0nF

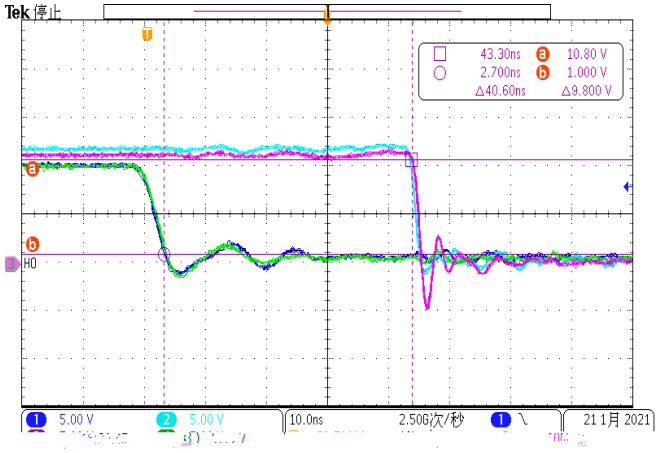


Figure 19. LO HO Falling Edge Propagation Delay, C_L=0nF

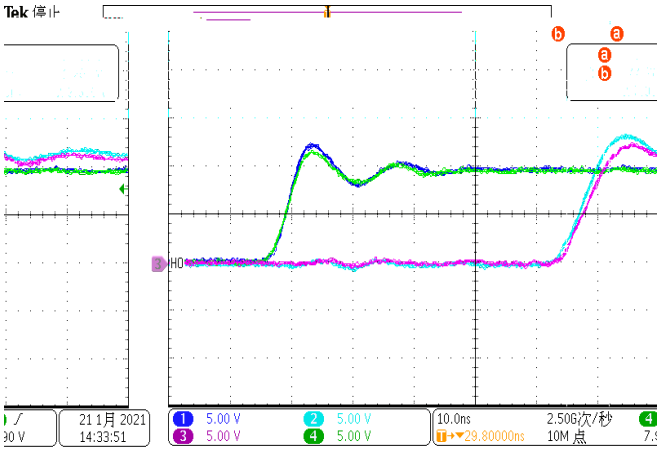


Figure 20. LO HO Rising Time, CL=1nF

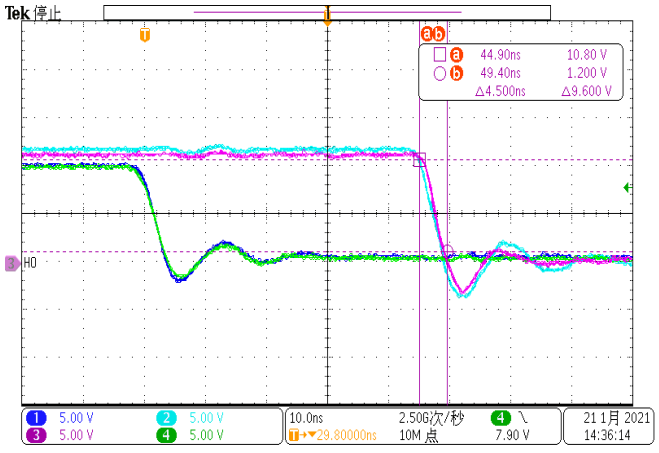


Figure 21. LO HO Falling Time, CL=1nF

Layout Guideline

1.

2.
3.

4.
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10.

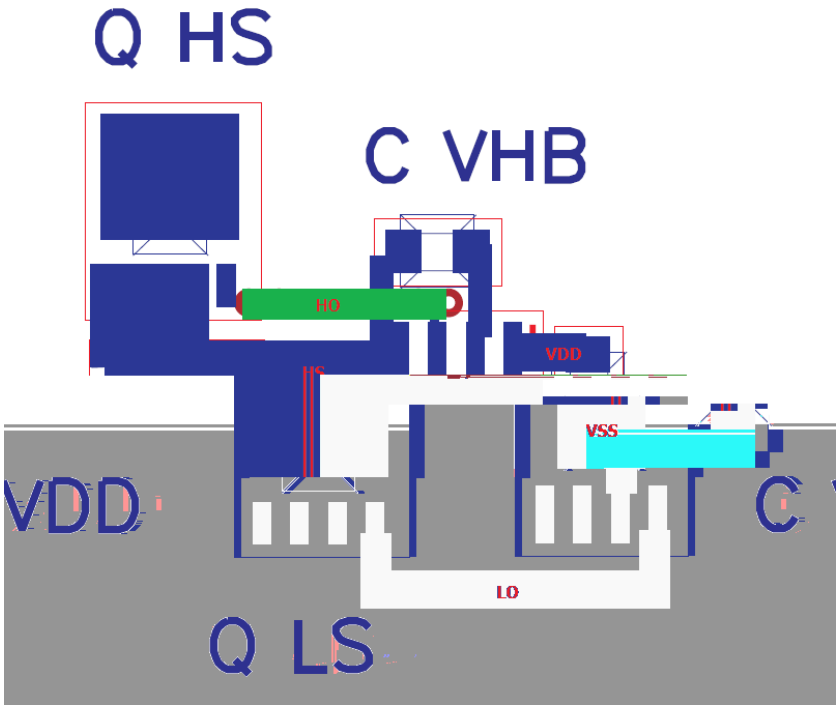
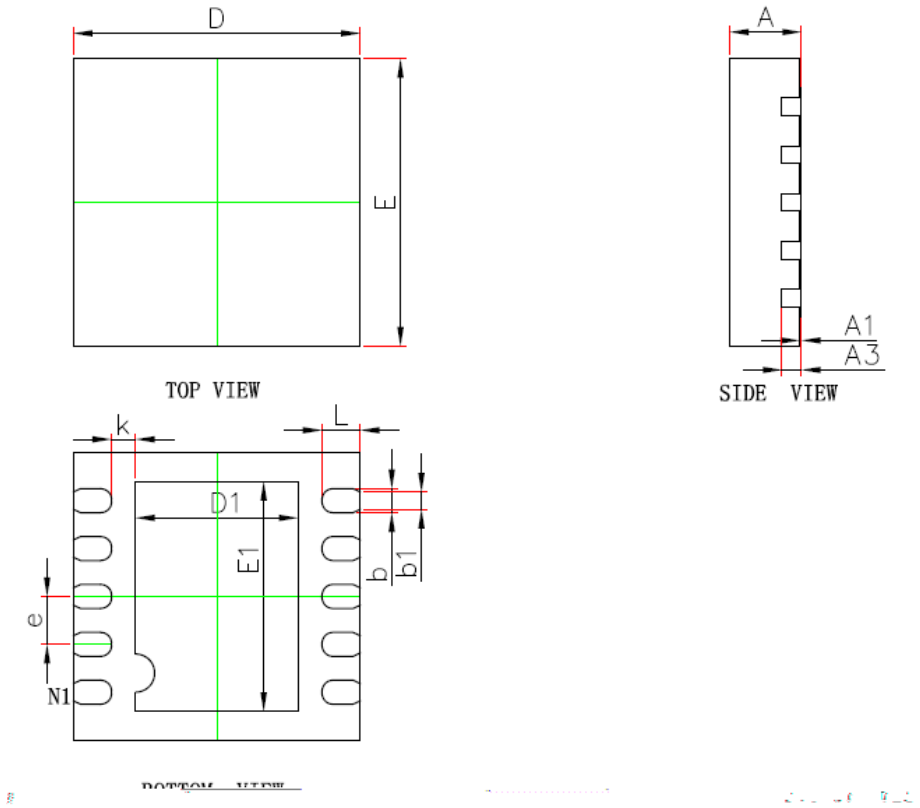


Figure 22. SCT52A40 PCB Layout Example



DFN3X3-10L Package Outline Dimensions

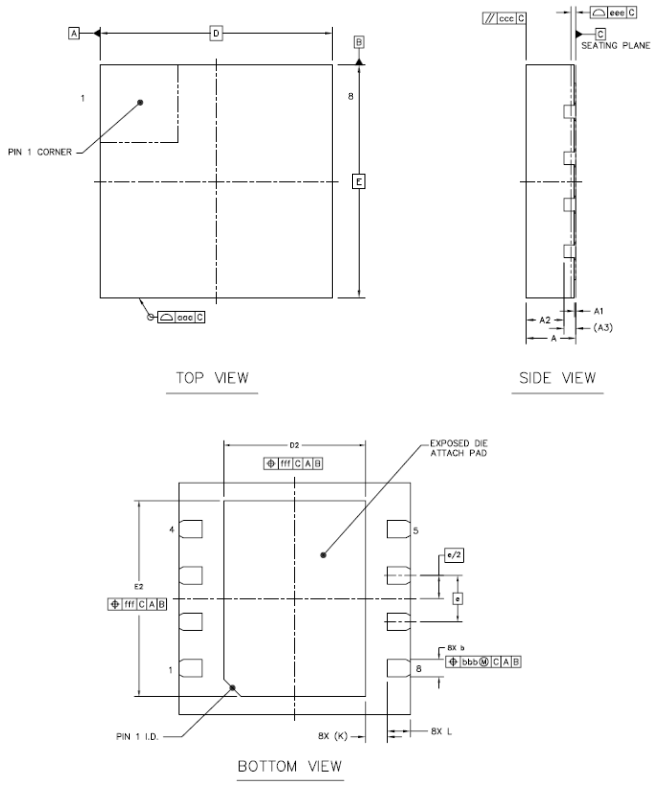
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF.		0.008 REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	1.600	1.800	0.063	0.071
E1	2.300	2.500	0.091	0.098
b	0.200	0.300	0.008	0.012
k	0.250 REF.		0.010 REF.	
b1	0.180 REF.		0.007 REF.	
e	0.500 BSC.		0.020 BSC.	
L	0.324	0.476	0.013	0.019

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

DFN3X3-9L Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.800	0.900	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF.		0.008 REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.300	1.500	0.051	0.059
E1	2.300	2.500	0.091	0.098
k	0.400 REF.		0.016 REF.	
b	0.200	0.300	0.008	0.012
b1	0.180 REF.		0.007 REF.	
e	0.500 BSC.			
LETQ				

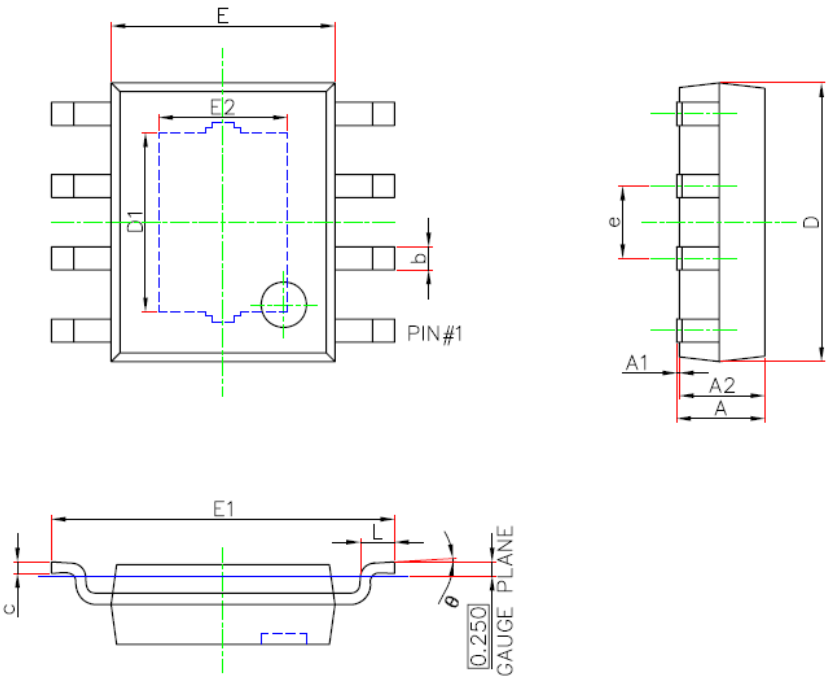


DFN4X4-8L Package Outline Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	---	0.65	---
A3		0.203 REF	
b	0.25	0.3	0.35
D	3.9	4	4.1
E	3.9	4	4.1
e		0.8 BSC	
D2	2.35	2.45	2.55
E2	3.28	3.38	3.48
L	0.3	0.4	0.5
K		0.375 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.1	
fff		0.1	

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

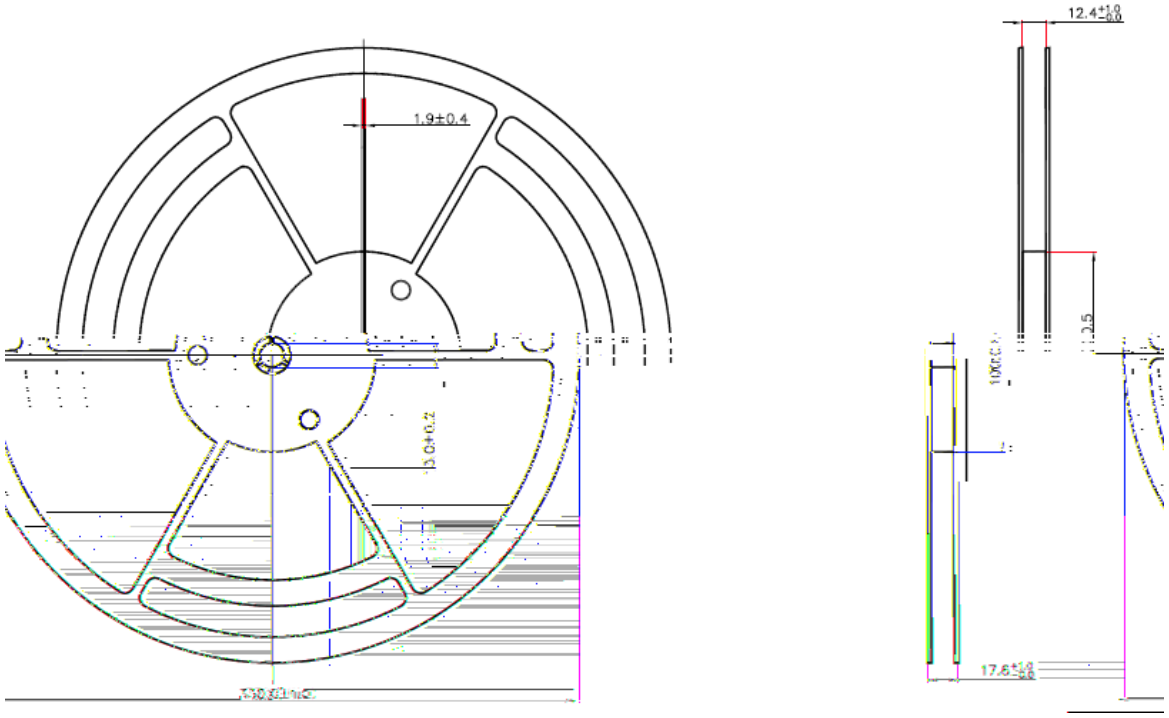


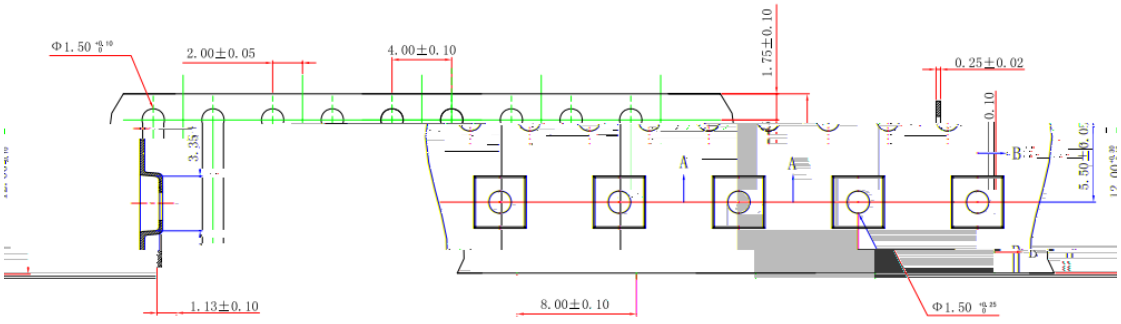
SOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

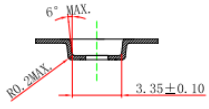
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.



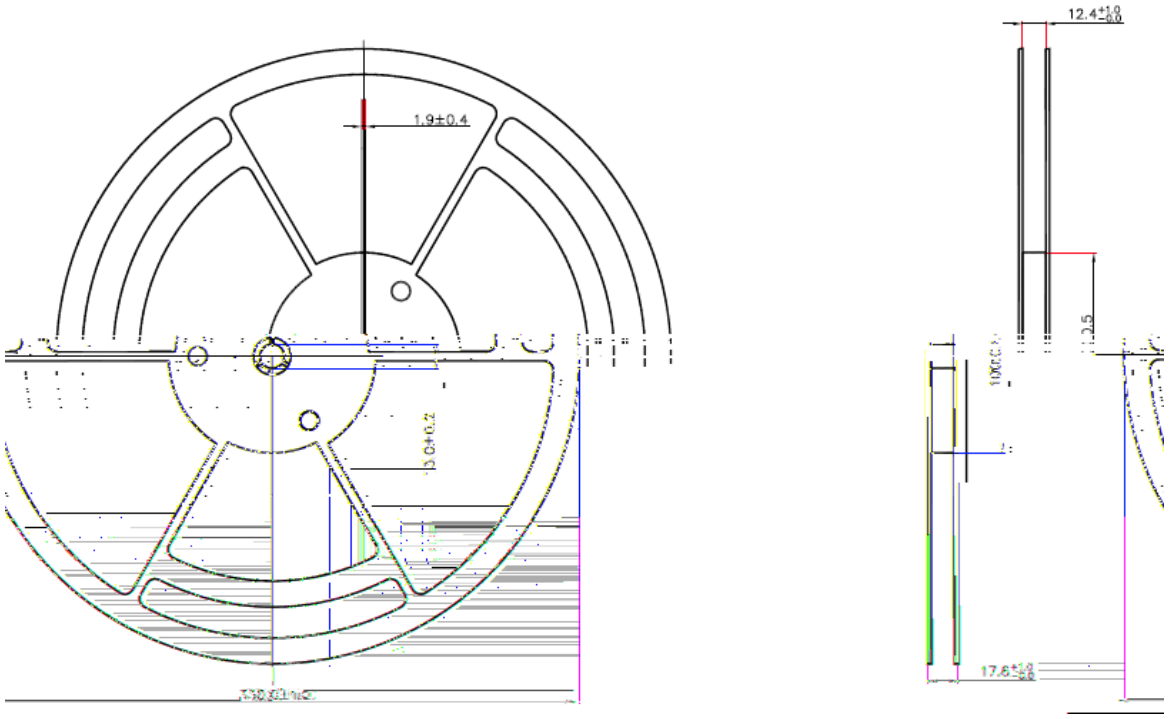


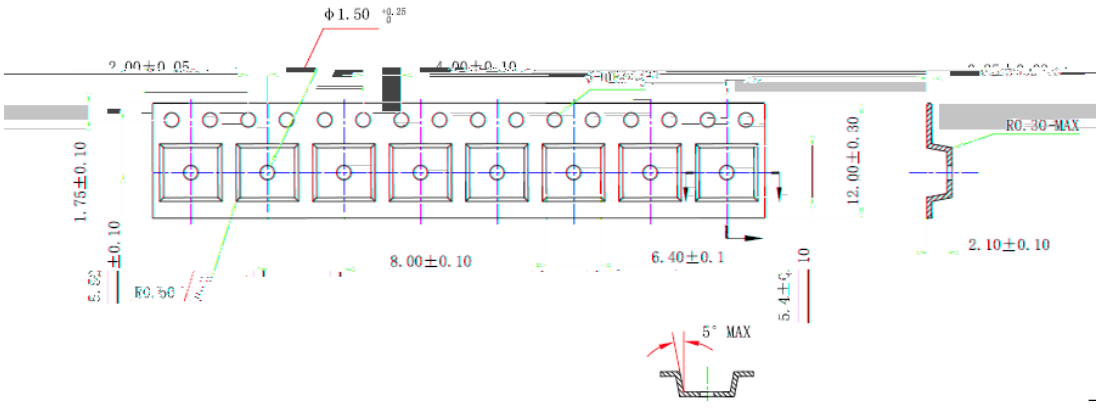
SECTION B-B



SECTION A-A

Feeding Direction





Feeding Direction

