40W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

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- VIN Input Voltage Range: 4.2V-30V
- PVIN Input Voltage Range: 1V~26V
- Up to 40W Power Transfer
- Integrated Full-Bridgefer

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update DEVICE ORDER INFORMATION and Description

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ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT63340FGAR	Tape & Reel	5000	3340	21	QFN-21L

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Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	32	V
PVIN1, PVIN2	-0.3	28	V
SW1,SW2	-1	28	V
SW3	-1	32	V
BST1,BST2	-0.3	34	V
BST3	-1	38	V
BST1-SW1,BST2-SW2,BST3-SW3	-0.3	6	V
VDD, V3P3, VDM, EN, PWM1, PWM2, ISNS, IDMO, VDMO, QDET	-0.3	6	V
Operating junction temperature TJ(2)	-40	125	°C
Storage temperature TSTG	-65	150	°C

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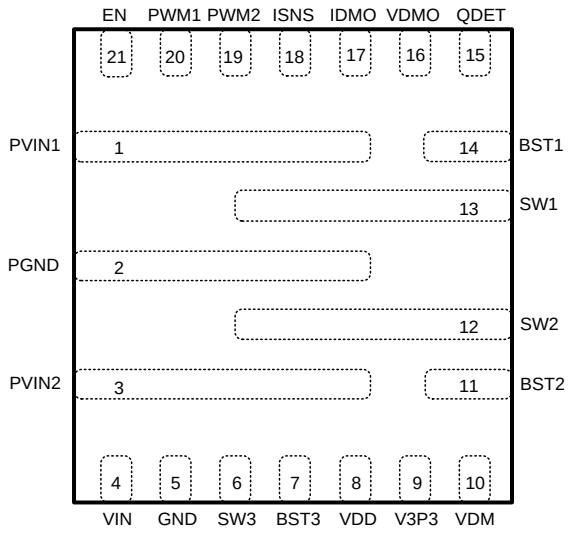

Figure 1. Top view 21-Lead QFN 4mm*4mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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NAME	NO.	PIN FUNCTION
PVIN1	1	Input supply voltage of half-bridge FETs Q1 and Q2. Connected to the drain of high side FET Q1. a local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
PGND	2	PGND is the common power ground of the full bridge, connected to the source terminal of low side FETs Q2 and Q4 internally.
PVIN2	3	Input supply voltage of half-bridge FETs Q3 and Q4. Connected to the drain of high side FET Q3. Local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.

VIN	4	Input supply voltage of the Buck converter. Add a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
GND	5	Power ground of the Buck converter.
SW3	6	Switching output of the Buck converter. Connect SW3 to an external power inductor.
BST3	7	Power supply bias for the high-side power MOSFET gate driver of Buck converter. Connect a 0.1uF capacitor from BST3 pin to SW3 pin.
VDD	8	Output voltage of the Buck converter. Connect 22uF capacitor from this pin to GND pin. VDD is also the input power supply for gate driver of power stage and the 3.3V LDO.
V3P3	9	3.3V LDO output. Connect 1uF capacitor to ground.
VDM	10	High-

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PARAMETER	THERMAL METRIC	QFN-21L	UNIT
R	Junction to ambient thermal resistance(1)	40	°C/W
R	Junction to case thermal resistance(1)	24	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63340 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63340. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DSON_L}	Low side FET on-resistance			250		
T_{SS}	Internal soft-start time			1.4		ms
3.3V LDO						
V_{3P3}	Output voltage	Cout=1uF, VDD=5V	3.267	3.3	3.333	V
I_{3P3}	Output current Capability			220		mA
I_{SC1}	Short current			40		mA
Current Sense						
V_{ISNS0}	Voltage with no input current	I_{PGND}=0A ,Tj=25 PWM1=PWM2=0V	0.585	0.6	0.615	V
R_{ISNS}	Input current to output voltage gain	$V_{ISNS}=V_{ISNS0}+I_{PGND}*R_{ISNS}$	0.98			

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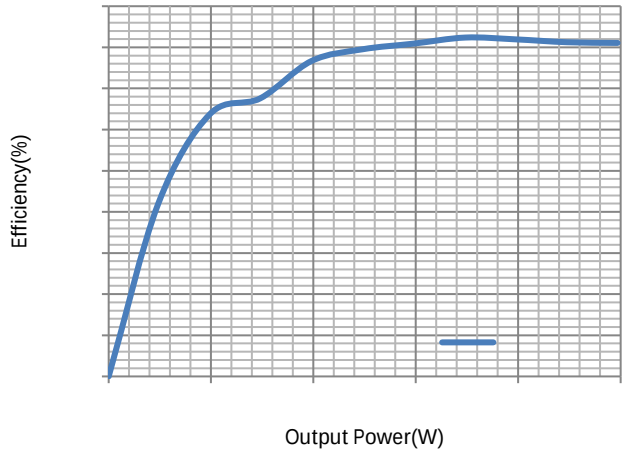

Figure 2.Transfer Efficiency with 5W RX@ Vout=5V

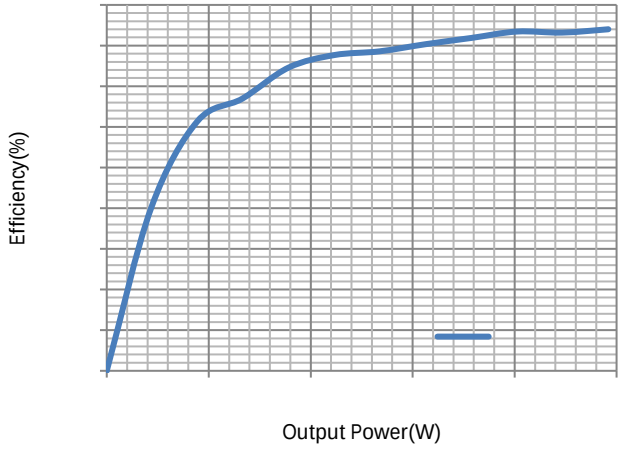

Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

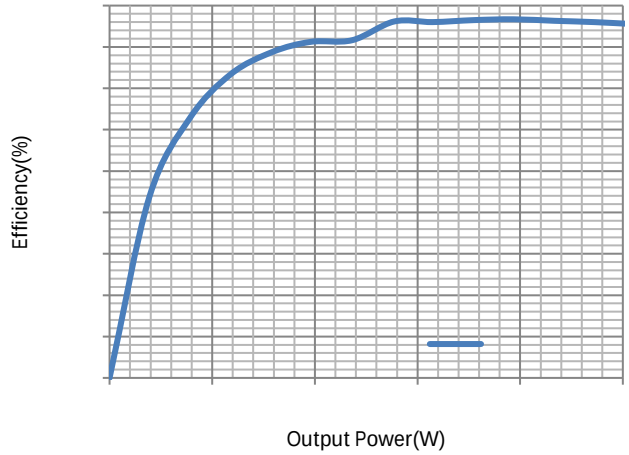

Figure 4. Transfer Efficiency with 15W RX@ Vout=12V

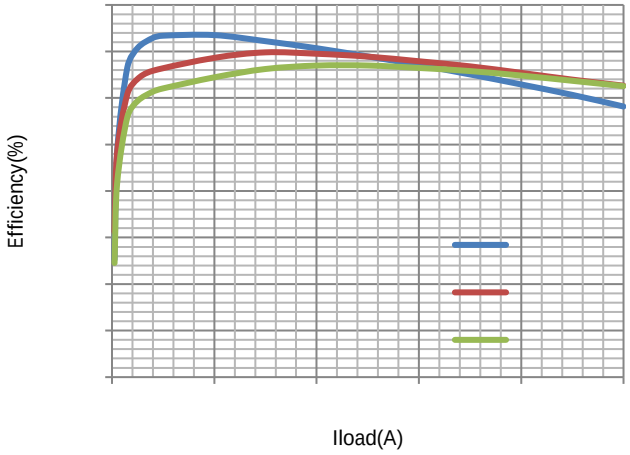

Figure 5. Buck Converter Efficiency

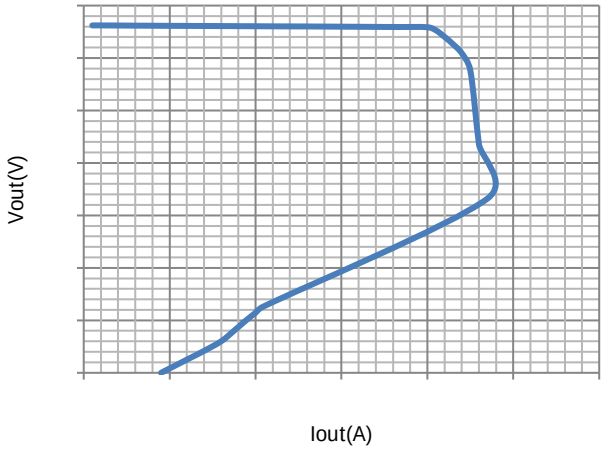

Figure 6. 3.3V LDO Iout vs Vout

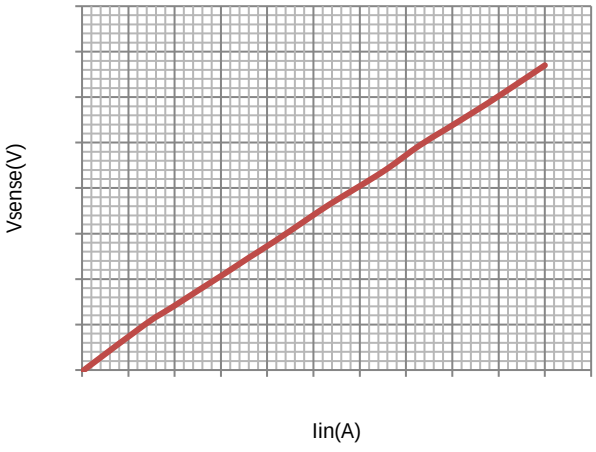

Figure 7. Current Sense Output Voltage vs Iin

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Overview

The SCT63340 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V buck converter as power supply for external transmitter controller and internal 5V power supply to increase system efficiency, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU.

The SCT63340 has four power input pins. VIN is connected to the power FETs of buck converter. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for transferring power. VDD is the output feedback pin of the 5V output buck converter meanwhile as the power supply for internal two LDOs and full bridge MOSFET's gate driver.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 30V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.2V typically. The maximum operating voltage for PVIN is up to 26V while the minimum voltage accepted can be down to1V. Another UVLO circuit also supervise the VDD voltage which is 93(V)-7(DD)- g0 G[ )]TJETQ /F45(ty)-M93 Tm0 g0 G[th)-8(e)-93(V)-7(DD)-

5V Output Buck Converter

The SCT63340fully integrates synchronous buck converter with up to 30V input voltage and 5V fixed output voltage, which offers up to 1A output current capability. The device employs 450KHz fixed frequency peak current mode control with the internal loop compensation network and built-in 1.4ms soft-start which makes this buck converter easily to be used by minimizing the off-chip component count. Pulse Skipping Modulation (PSM) is adopted to increase the light load efficiency.

The buck converter's output, a fixed 5V voltage, supports the power requirement on system such as transmitter controller or mechanical fan meanwhile it is also the power supply of the SCT63340's 3.3V LDO and gate drivers of 4-MO6( )MCID 79/Lang (e0009m37(oE009(n)4)5(s)-5(o/Span <MCID 80/Lang (en-US)>BDC q0.00000912 0 612 792 reW* n

Full Bridge Over Current Protection

The SCT63340 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 12.5A typical, the high side FET turns off immediately in present cycle to avoid current increasing further even that PWM signal still stays in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

Current Sense

The SCT63340 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with ±2% accuracy and reports a proportional voltage directly to the ISNS pin. This voltage information on ISNS pin can be sent to application specific controller ASIC or general MCU for Foreign Object Detection FOD and current demodulation.

When the full bridge of MOSFETs does not work, no current flows to PGND. The DC bias voltage on ISNS pin is 600mV.This DC bias helps set up a suitable voltage bias for the following analog to digital converter in MCU or amplifier for current demodulation. The average input current to voltage conversion gain on ISNS is 1V/A. The equation 3 represent the corresponding relation for the output voltage on ISNS pin and average current to PGND from full bridge.

$$V_{ISNS} = 600mV + I_{PGND} * 1V/A \qquad (3)$$

3.3V LDO

The SCT63340 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 200mA.This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Q Factor Detection

The SCT63340 integrated a low cost, reliable Q factor detection circuit to assure foreign objects detection before the selection phase. It generates a small pulse to detect any foreign object on the transmitter coil, it can detect metal on the transmitter coil easily.

After chip enable, apply a low voltage level pulse to EN pin can trigger the Q factor detection feature. The pulse width should be longer than 50us but less than 200us. SW1 will be preset to 2V for 4.7ms and then pull low to ground and this apply power to LC resonant loop and Vcoil will appear damping oscillation after SW1 short to ground. The SCT63340 will generate a pulse on VDMO pin and MCU can capture this pulse to calculate the Q factor by the pulse width as the Equation 4 shows. PWM1 and PWM2 should be low in Q factor detection phase.

$$Q = \frac{\triangle T * \pi}{10 * \ln \frac{V_{TH\_HIGH}}{V_{TH\_LOW}}} \qquad (4)$$

where

- ΔT is the pulse width on VDMOS pin
- V_{TH_HIGH} is high threshold 0.2V
- V_{TH_LOW} is low threshold 0.1V

Voltage and Current Demodulation

The SCT63340 integrates two demodulation schemes, one based on coil voltage information calling voltage demodulation and the other based on input average current information calling current demodulation.

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Typical Application

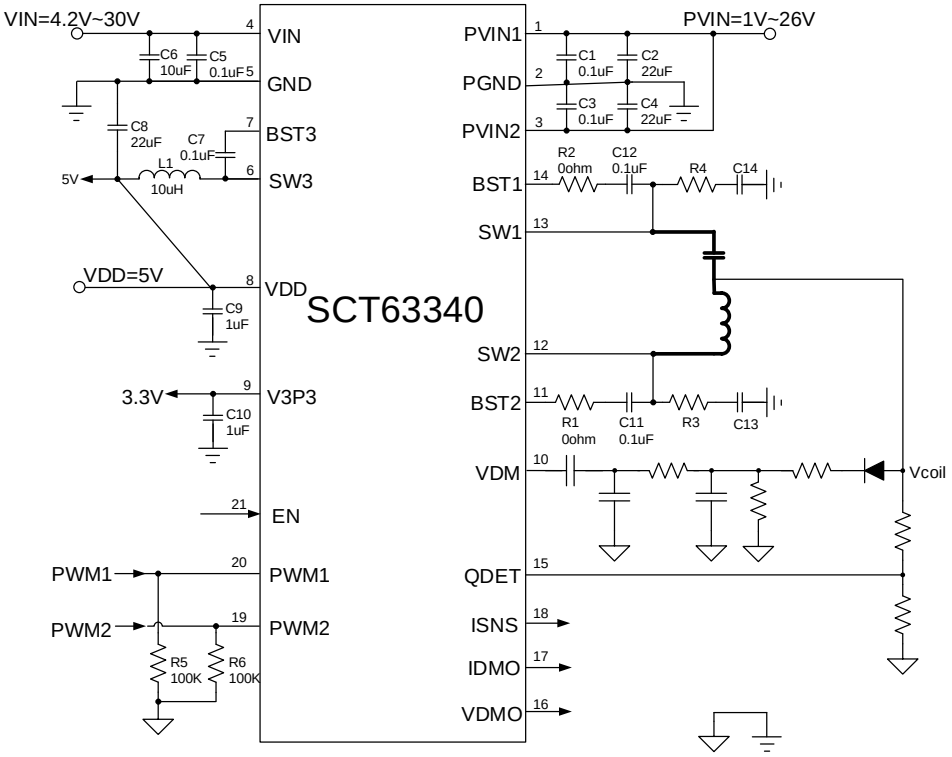

Figure 11. Separate Input to VIN and PVIN

Application Waveforms

Figure 12. Power Up

Figure 13. Power Down

Layout Guideline

Proper PCB layout is a critical for SCT63340
currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Buck converter output capacitor's ground should connect to GND directly to minimize the power loop.
5. VDD pin can connect to the DC/DC's output capacitor from bottom layer, connect to the point behind the capacitor while not connect to inductor.
6. Bypass capacitor for VDD place next to VDD pin.
7. Bypass capacitor for V3P3 place next to V3P3 pin.

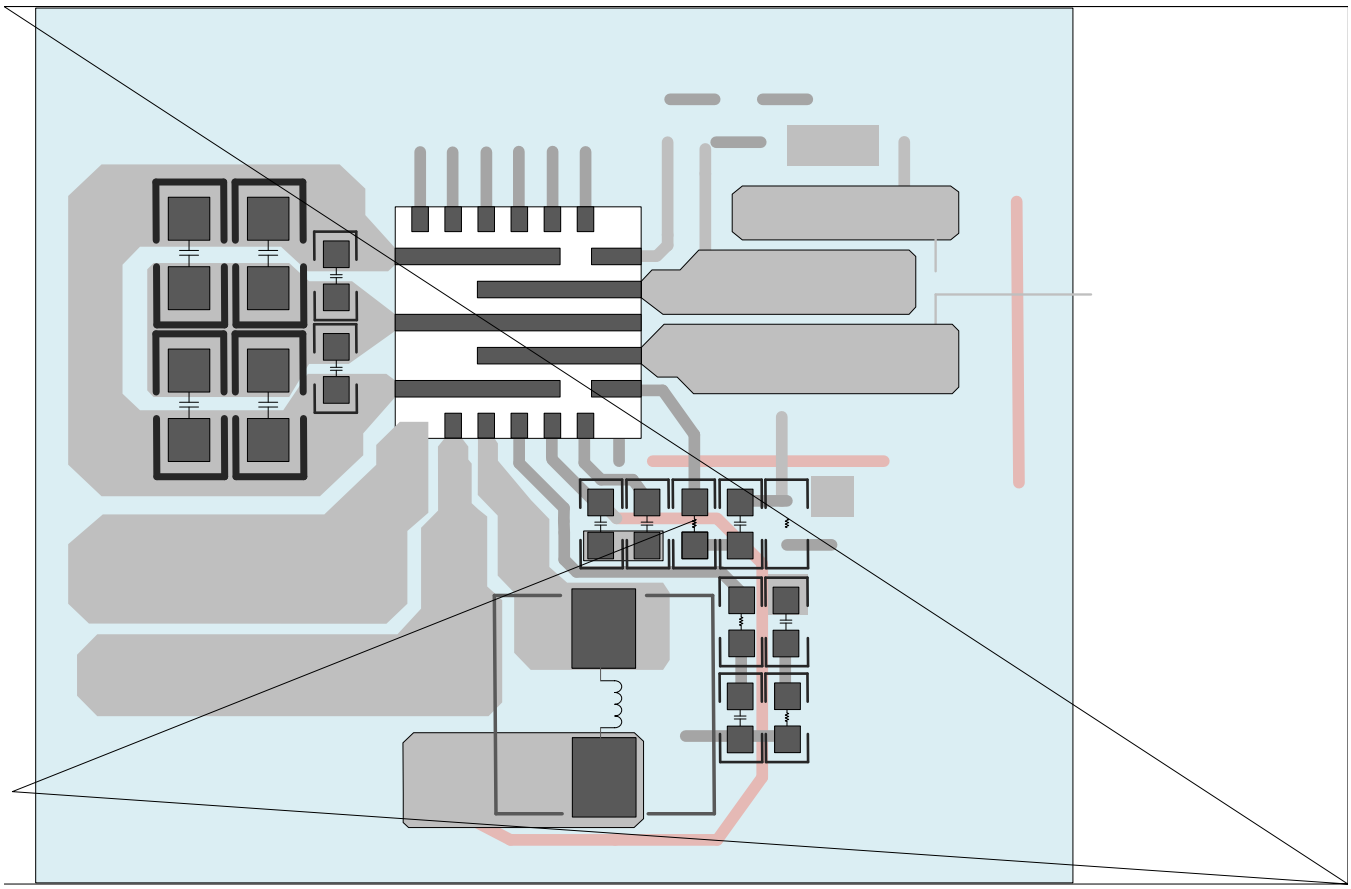

Figure 18. PCB Layout Example

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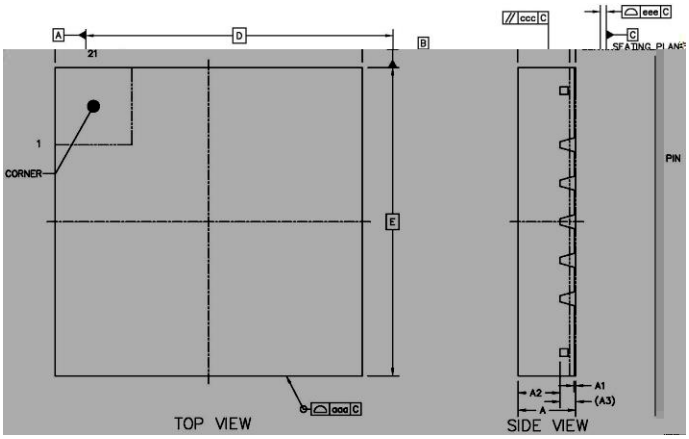

FCQFN-21L (4x4) Package Outline Dimensions

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
[illegible]TH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		1 BSC	
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.75	0.85	0.95
		L2	2.65	2.75	2.85
		L3	2.8	2.9	3
[illegible] EDGE TOLERANCE					

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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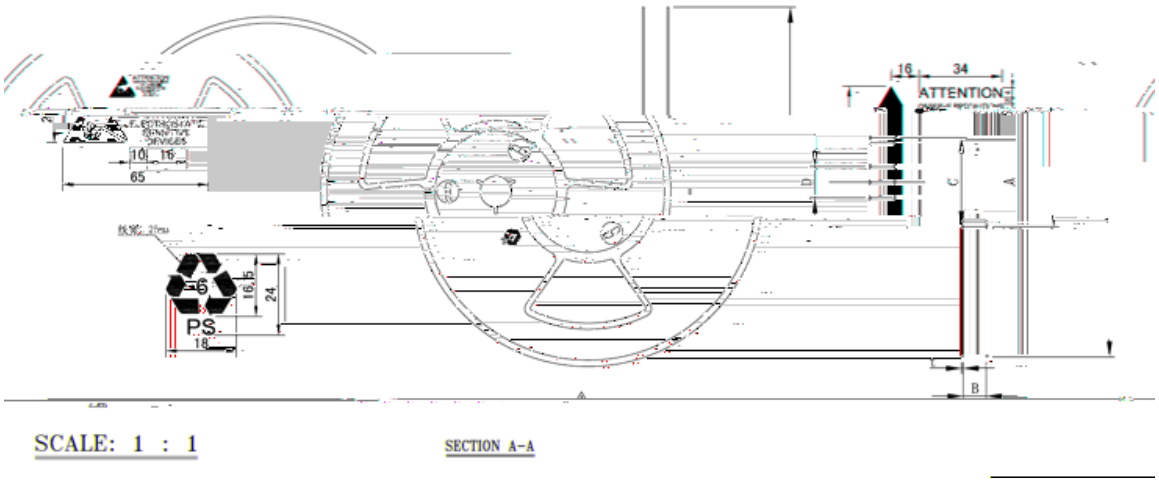
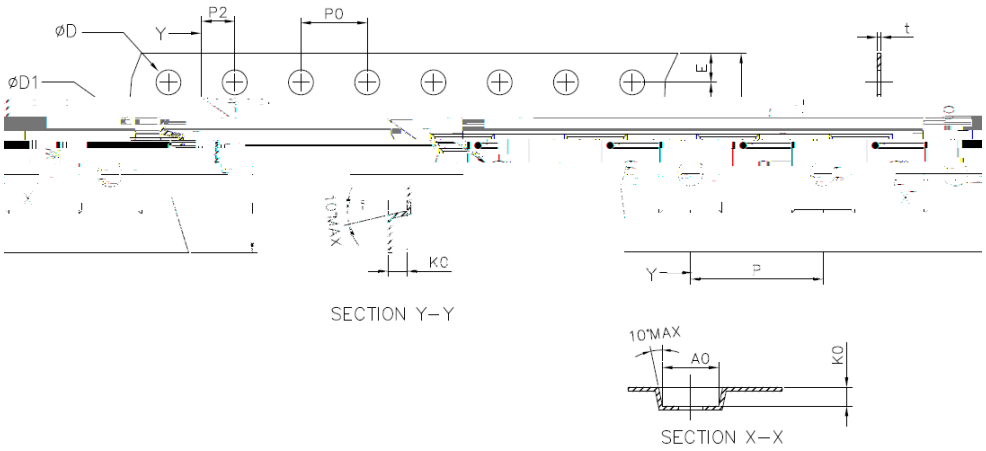


REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3



TAPE DIMENSIONS

W (mm)	A0 (mm)	B0 (mm)	K0 (mm)	t (mm)	P (mm)
$^{+0.30}_{-0.10}$	3.40±0.10	4.40±0.10	1.14±0.10	0.25±0.02	8±0.10

E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)
1.75±0.10	5.50±0.05	2.00±0.05	$^{+0.10}_{0}$	$^{+0.25}_{0}$	4.00±0.10	40.0±0.20

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PN	DESCRIPTION	COMMENTS
SCT63240	Up to 20W High Integration High Efficiency PMIC for Wireless Power Transmitter	