Ideal Diode Controller with Reverse-Current Protection

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device CDM ESD Classification Level C3B
- 4.8V to 65V Operating Range
- –65V Reverse voltage rating
- Charge pump for external N-Channel MOSFET
- 20mV ANODE to CATHODE forward voltage drop regulation
- 12V Gate Drive Voltage
- With Enable Input
- Drive High Side External N-Channel MOSFET
- 1μA Shutdown current (EN=Low)
- 60μA Operating quiescent current (EN=High)
- 2.3-A Peak gate turnoff current
- Fast reverse current turn-off within 0.75us
- Meets automotive ISO7637 transient requirements with a suitable TVS Diode
- Available in an SOT23-6L Package

APPLICATIONS

- Automotive Battery Protection
- Redundant Power Supplies
- Industrial Factory Automation
- Enterprise Power Supplies
- Network Telecom Power Systems
- Servers

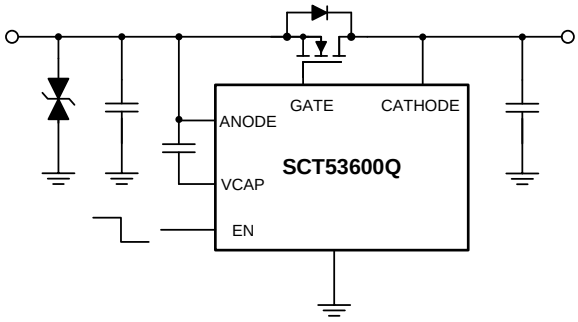
DESCRIPTION

The SCT53600Q is an ideal diode controller which paired with an external N-channel MOSFET as an ideal diode rectifier for low loss reverse polarity protection to replace a Schottky Diode. The SCT53600Q operates over a wide supply voltage range of 4.8V to 65V. The device can withstand and protect the load against damaging from negative supply voltages down to –65 V and blocks reverse current flow helping to simplify the system designs for automotive ISO7637 protection.

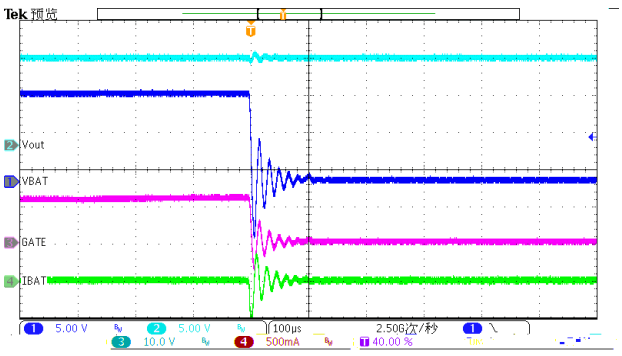
The SCT53600Q controller provides a charge pump gate drive for an external N-channel MOSFET. The device regulates the forward voltage drop across the external MOSFET to 20mV allowing smooth, ring-free operation with providing very fast turn-off(< 0.75 μs) of the MOSFET during a reverse event to minimize reverse current if power source fails or input micro-short conditions. The fast response to Reverse Current Blocking makes the device suitable for systems with output voltage holdup requirements during ISO7637 pulse testing.

The SCT53600Q consumes only 1μA of current during shutdown mode with the enable pin low to extend battery life. The device is available in an SOT23-6 package.

TYPICAL APPLICATION



Typical Application



Reverse Current Blocking

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Production.

Revision 1.1 Update $I_{Q\_Charge\ On}$ MAX and MIN.

Revision 1.2 Modify part number .

Revision 1.3 Update packaging information

Revision 1.4: Update Device Order Information

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT53600TVDR	Tape & Reel	3000	3600	6	SOT23-6L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
ANODE to GND	-65	65	V
EN to GND, $V_{(ANODE)}$ > 0 V	-0.3	72	V
EN to GND, $V_{(ANODE)}$ ≤ 0 V	$V_{(ANODE)}$	65+ $V_{(ANODE)}$	V
GATE to ANODE	-0.3	15	V
VCAP to ANODE	-0.3	15	V
CATHODE to ANODE	-5	75	V
Operating junction temperature TJ(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

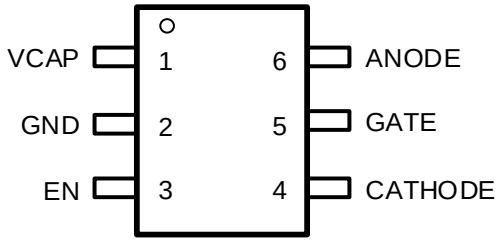


Figure 1. 6-Lead Plastic SOT23-6L

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
VCAP	1	Charge pump output. Connect a charge pump capacitor typically 0.1uF between VCAP and ANODE.
GND	2	Ground.
EN	3	Enable pin. Drive EN low to make the device in shutdown mode. Can be connected to ANODE for always ON operation.
CATHODE	4	Cathode of the diode. Connect to the drain of the external N-channel MOSFET.
GATE	5	Gate drive output. Connect to the gate of the external n-channel MOSFET. GATE shorts to ANODE during reverse-current conditions and when EN is forced low.
ANODE	6	Anode of the diode and input power. Connect to the source of the external N-channel MOSFET.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
$V_{(ANODE)}$	ANODE to GND	-60	60	V
$V_{(CATHODE)}$	CATHODE to GND		60	V
V_{EN}	EN to GND	-60	60	V
$V_{(ANODE)}$ -$V_{(CATHODE)}$	ANODE to CATHODE	-70		V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-3	3	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	SOT23-6L	UNIT
	Junction-to-ambient thermal resistance (standard board)	102	°C/W
	Junction-to-case (top) thermal resistance	36.9	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2601 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2600. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(ANODE)}$	Operating input voltage		4.8		60	V
$V_{(ANODE\ POR)}$	VANODE POR Rising threshold			4.3	4.75	V
	VANODE POR Falling threshold			3.7		V
I_{SHDN}	Shutdown current	V_{EN}= 0V		0.3	1.5	μA
$I_{Q\_Charge\ Off}$	Quiescent current	Vcap-ANODE=14V		60	130	uA
$I_{Q\_Charge\ On}$	Quiescent current	Vcap-ANODE Floating	180	285	650	uA
ENABLE						
V_{EN_H}	Enable input high threshold			2.15		V
V_{EN_L}	Enable input low threshold			1.48		V
V_{EN_HYS}	Enable Hysteresis			0.65		V
I_{EN}	Enable sink current	V_{EN} = 12 V		1.5		uA

V_{ANODE} to $V_{CATHODE}$						
V_{AC_REG}	Regulated Forward Threshold	TJ=25	11	20	29	mV
		TJ=40~125	7		36	
V_{AC}	threshold for full conduction mode			50		mV
V_{AC_REV}	threshold for reverse current blocking	TJ=40~125	-30	-11	-1	mV
Gm	Regulation Error AMP Transconductance*			1800		µA/V
GATE DRIVE						
I_{GATE}	Peak source current	$V_{ANODE} – V_{CATHODE}$ = 100 mV, $V_{GATE)} – V_{ANODE}$ = 5 V		7		mA
	Peak sink current*	$V_{ANODE} – V_{CATHODE}$ = –20 mV, $V_{GATE} – V_{ANODE}$ = 5 V		2370		mA
	Regulation max sink current	$V_{ANODE} – V_{CATHODE}$ = 0 V, $V_{GATE} – V_{ANODE}$ = 5 V		12		uA
R_{DSON}	discharge switch R_{DSON}	$V_{ANODE} – V_{CATHODE}$ = –20 mV,				

TYPICAL CHARACTERISTIC

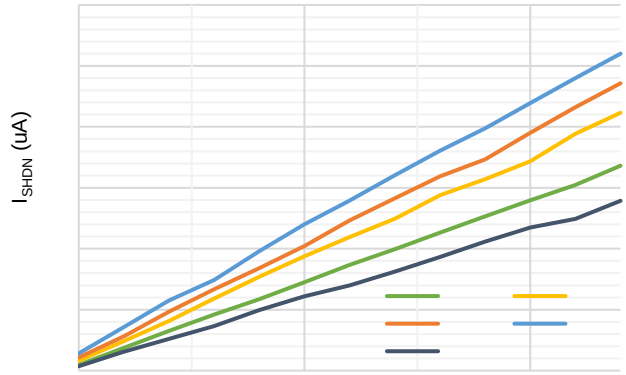


Figure 2. Shutdown Supply Current vs Supply Voltage

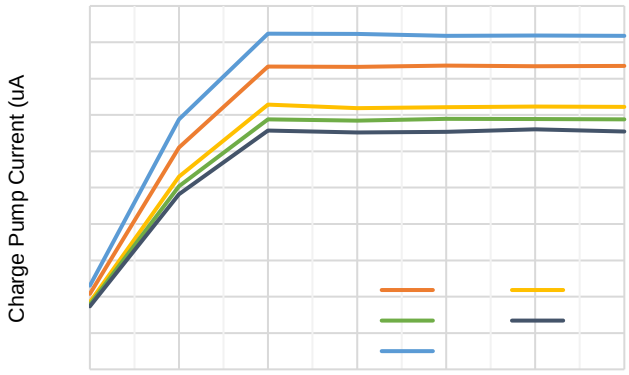


Figure 3. Charge Pump Current vs V_{ANODE} at VCAP= 6 V

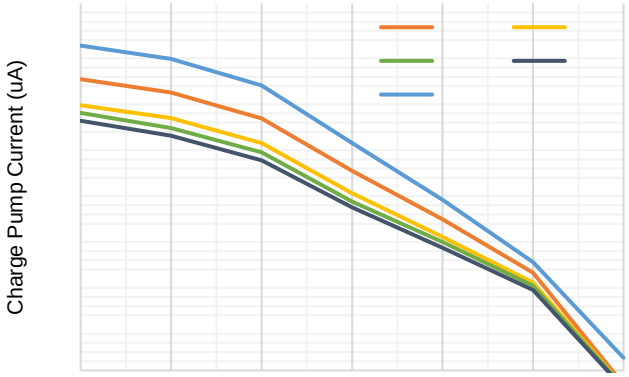


Figure 4. Charge Pump V-I at VANODE >= 12V

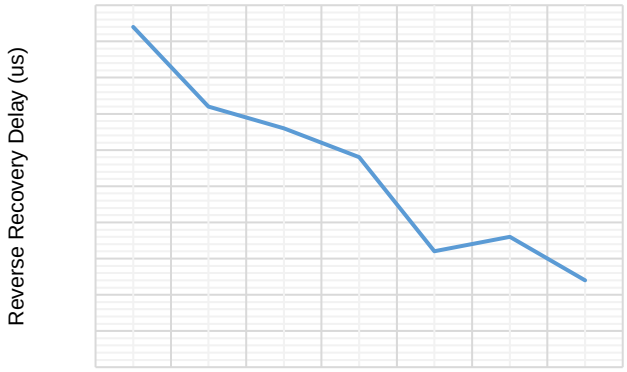


Figure 5. Reverse Current Blocking Delay vs Temperature

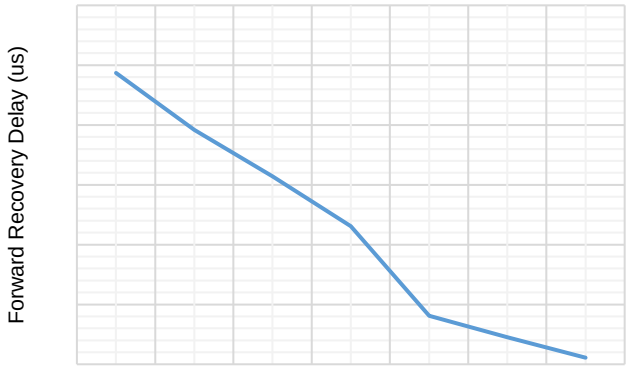


Figure 6. Forward Recovery Delay vs Temperature

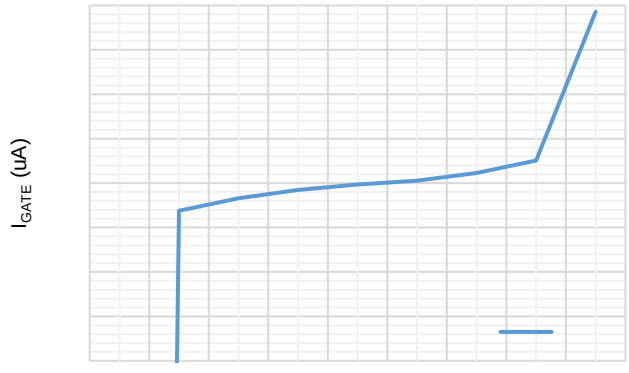


Figure 7. Gate Current vs Forward Voltage Drop

FUNCTIONAL BLOCK DIAGRAM

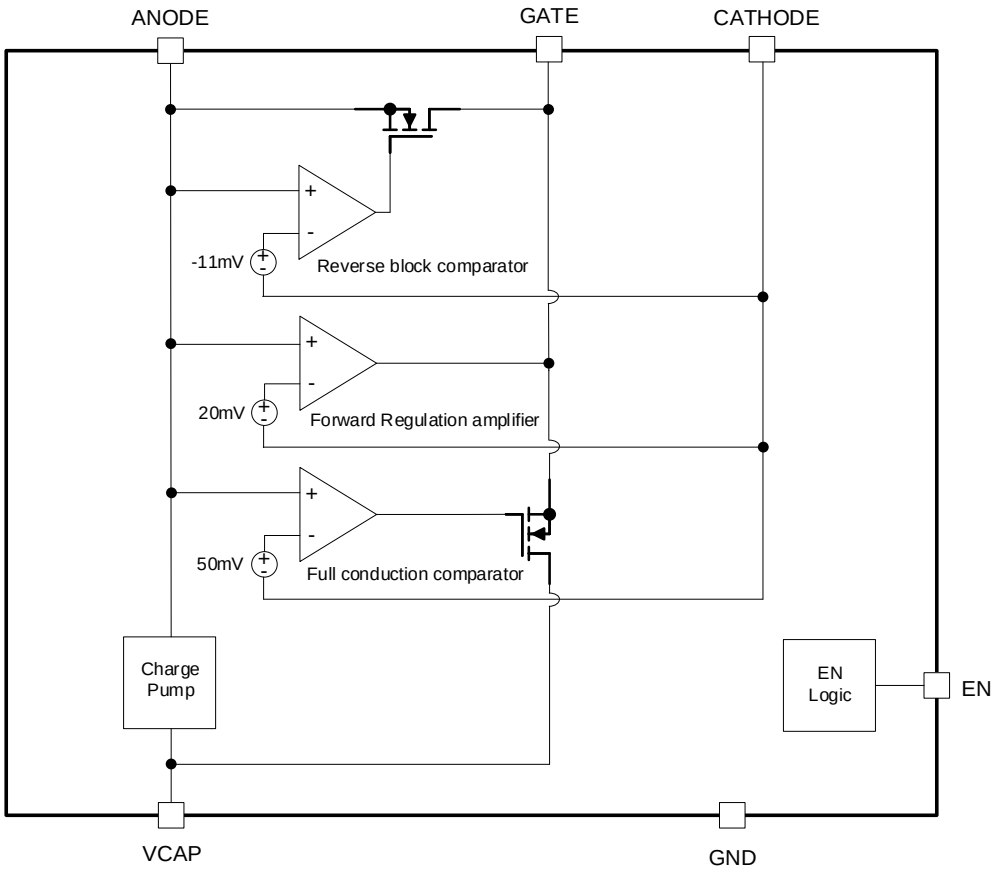


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT53600Q is a high-voltage, ideal diode controller that provides system protection against reverse voltage, reverse-current flow, and destructive automotive transient voltages to implement an efficient and fast reverse polarity protection circuit or be used in a redundant power system. This easy to use ideal diode controller operates in conjunction with an external N-channel MOSFET to replace other reverse polarity schemes such as a P-channel MOSFET or a Schottky diode.

The SCT53600Q controller provides a charge pump gate drive for an external N-channel MOSFET. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20 mV. This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below –11 mV, resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. The fast response to Reverse Current Blocking makes the device suitable for systems with output voltage holdup requirements during ISO7637 pulse testing.

The SCT53600Q consumes only 0.3µ

The SCT53600Q operate in **full conduction mode** if the current from source to drain of the external MOSFET be large enough to result in an ANODE to CATHODE voltage drop of greater than 50 mV typical. The GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFET's RDS(ON) is minimized reducing the power loss of the external MOSFET when forward currents are large.

The SCT53600Q operate in **reverse current protection mode** if the ANODE to CATHODE voltage is typically less than –11 mv. The GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

The SCT53600Q operate in **forward regulation mode** if the current from source to drain of the external MOSFET be within the range to result in an ANODE to CATHODE voltage drop of –11 mV to 50 mV. During forward regulation mode the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. This closed loop regulation scheme enables graceful turn off of the MOSFET at very light loads and ensures zero DC reverse current flow.

APPLICATION INFORMATION

Typical Application- Reverse Polarity Protection

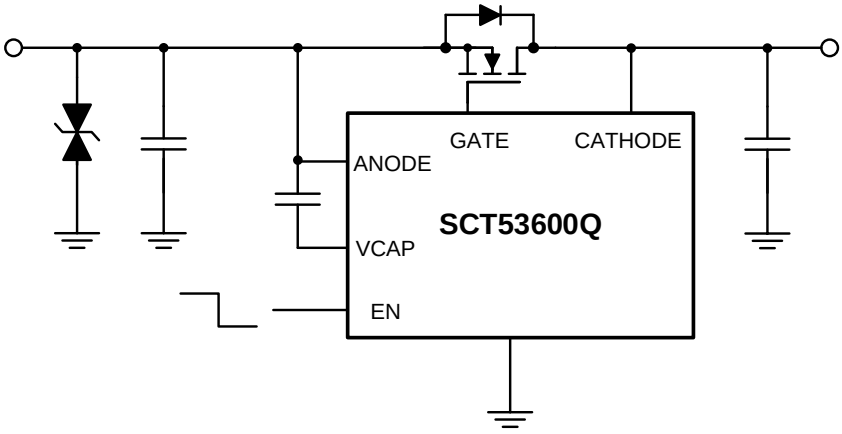


Figure 9. Typical 12V Battery Protection with single bi-directional TVS

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Battery, 12V Nominal with 35V Load Dump
Output Voltage	4.8V during Cold Crank to 35V Load Dump
Output Current Range	3A Nominal, 5A Maximum
Output Capacitance	1 µF Minimum, 47 µF Typical Hold Up Capacitance

MOSFET Selection

MOSFET selection is critical to designing a proper protection circuit. Several factors must be considered: gate capacitance, maximum continuous drain current I_D, maximum drain-to-source voltage rating, on-resistance $R_{DS(ON)}$, maximum source current through body diode, peak power dissipation capability and the average power dissipation limit. Gate capacitance is not as critical, but it does determine the length of turn-on and turn-off times. MOSFETs with more gate capacitance tend to respond more slowly.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen

Application Waveforms

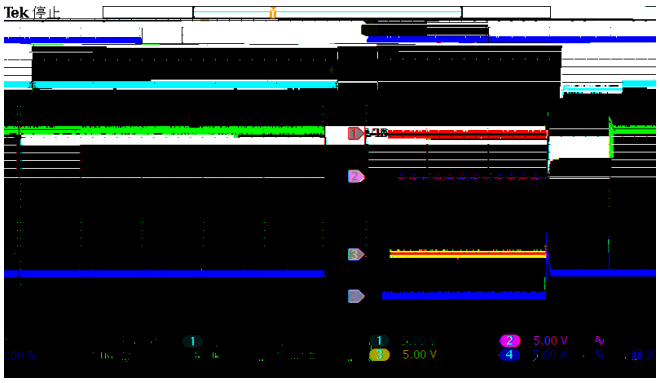


Figure 10. Start up with 3A load

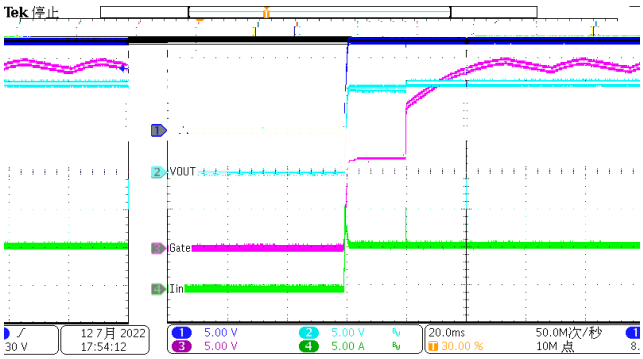


Figure 11. Start up with 5.8A load

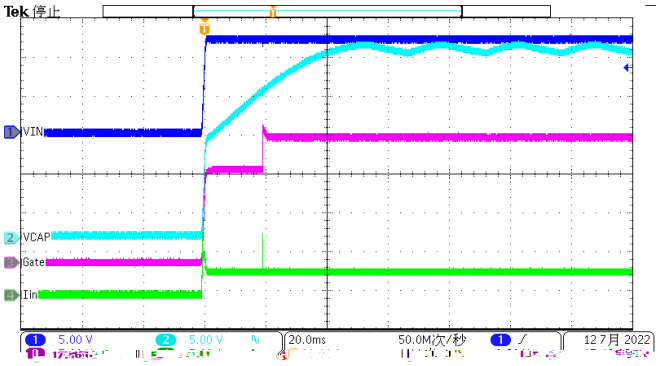


Figure 12. VCAP during startup at 3A load

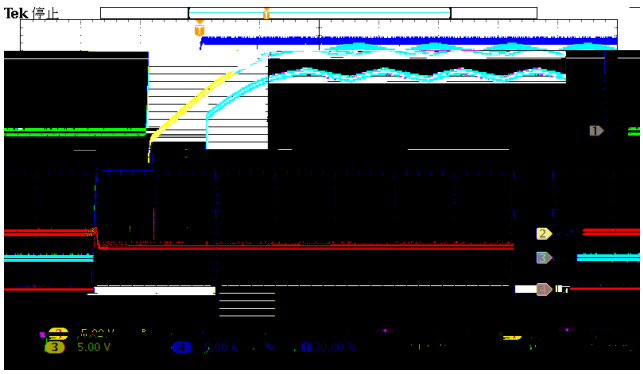


Figure 13. VCAP during startup at 5.8A load

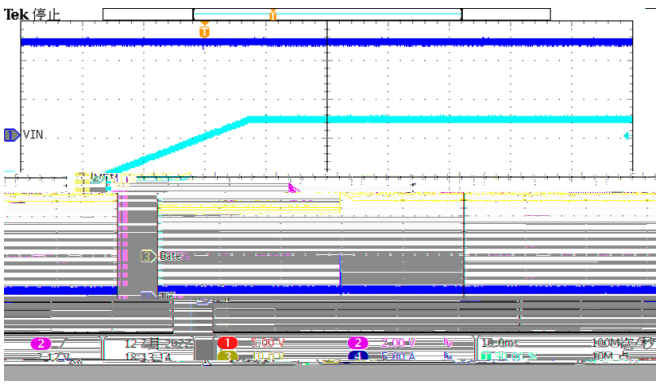


Figure 14. Enable Threshold

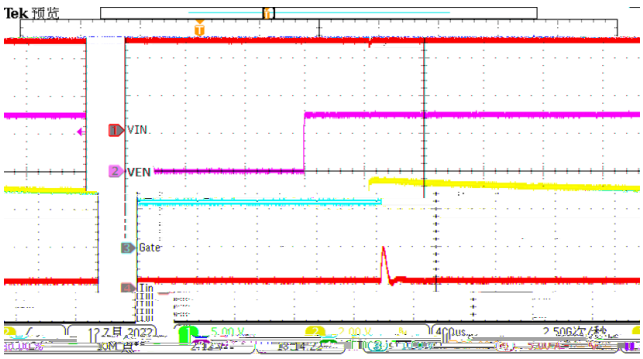


Figure 15. Enable turn on delay

Application Waveforms(continued)

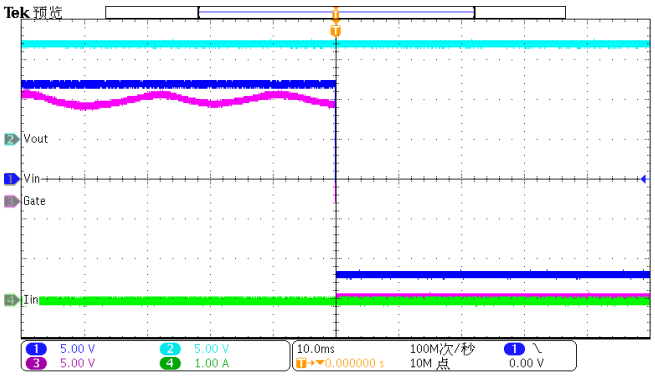


Figure 16. Static Reverse Polarity

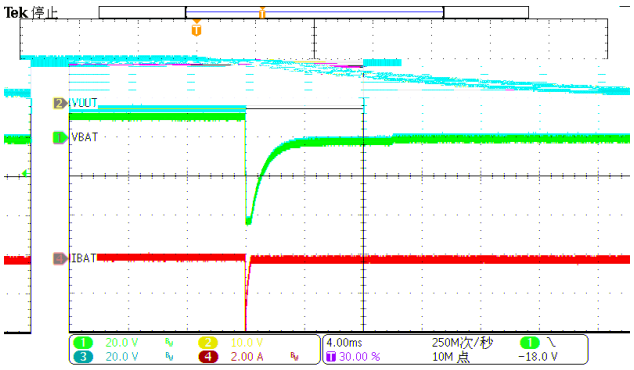


Figure 17. Dynamic Reverse Polarity(ISO 7637-2 Pulse 1)

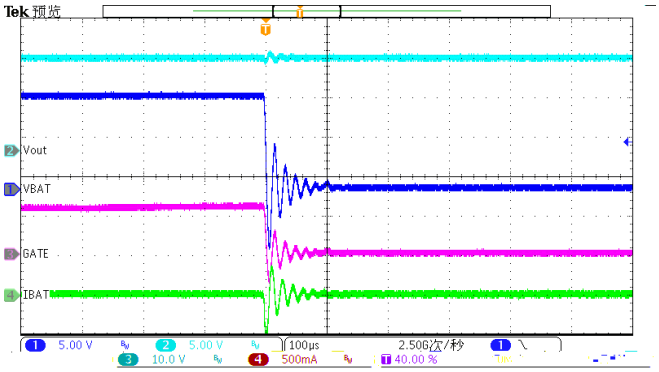


Figure 18. Input Short Response

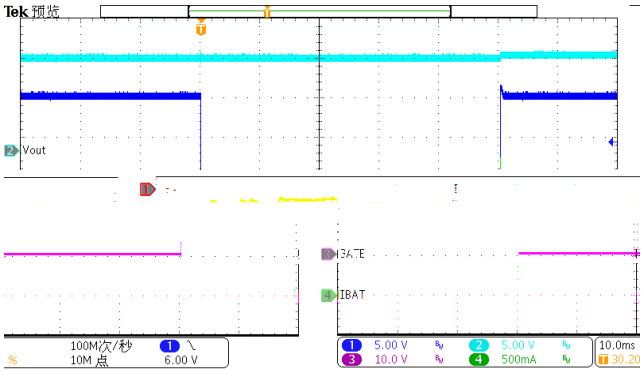


Figure 19. Input Micro-Short

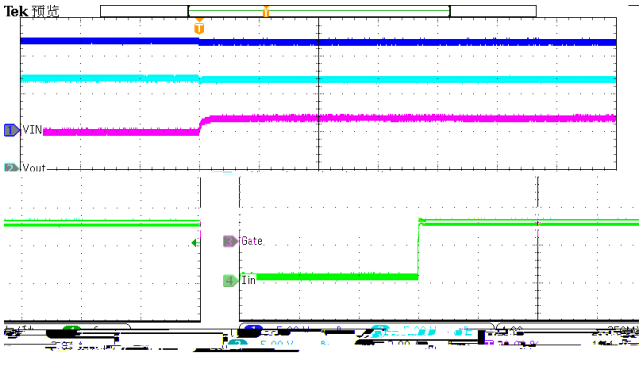


Figure 21. Load Transient Response, 0.1A->3A

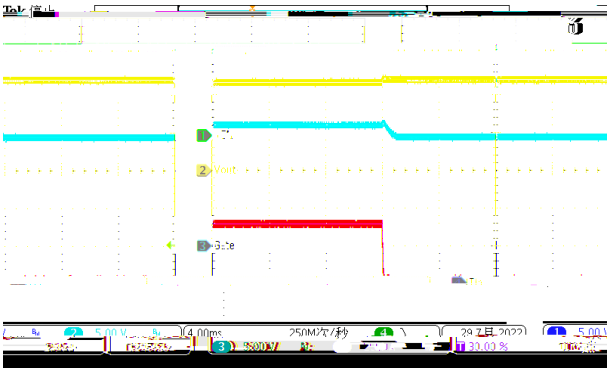


Figure 21. Load Transient Response, 3A->0.1A

APPLICATION INFORMATION

Typical Application- Redundant Power

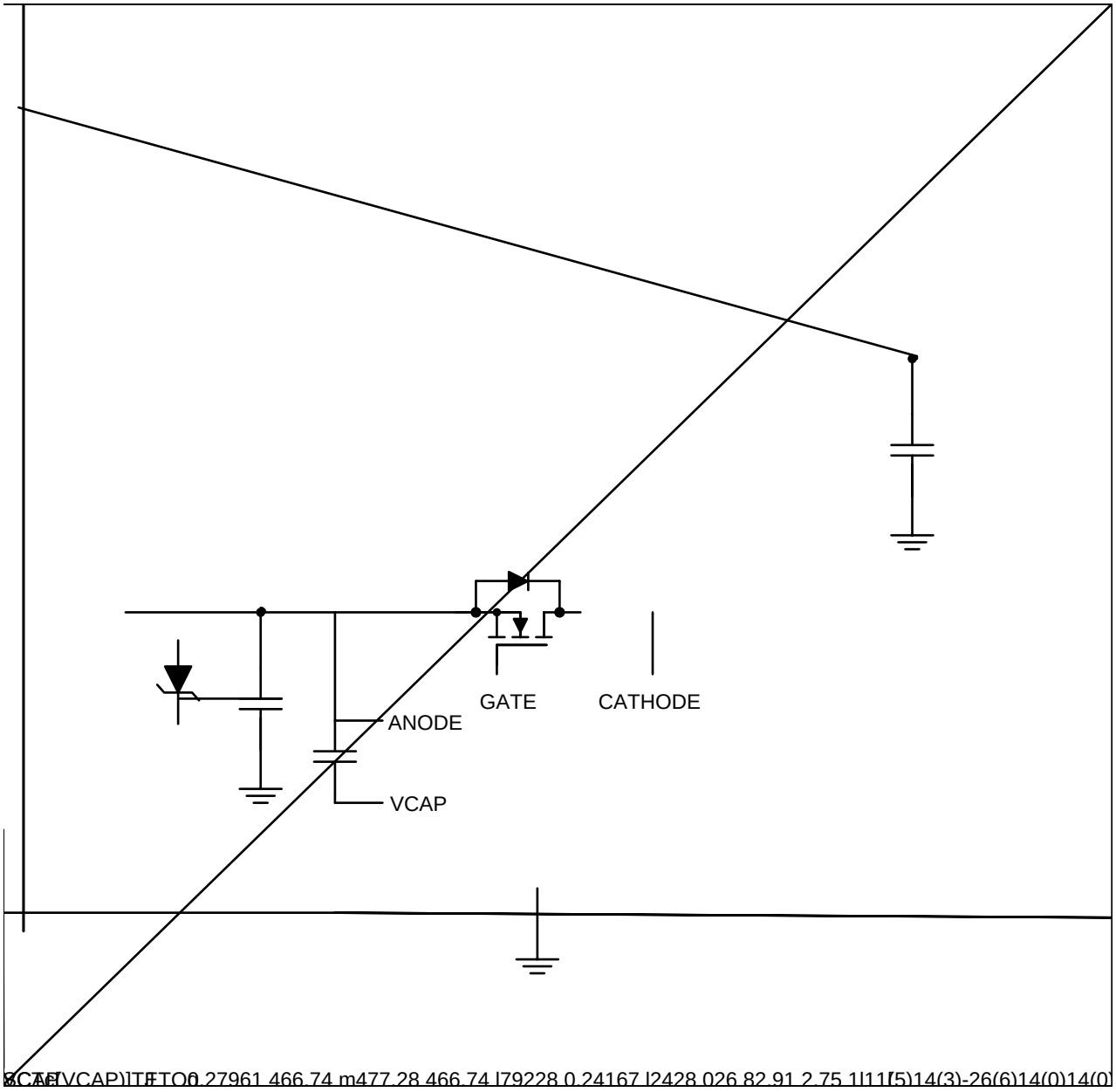


Figure 22. Redundant Power Supply Application

Layout Guideline

1. Connect ANODE, GATE and CATHODE pins of SCT53600Q close to the MOSFET's SOURCE, GATE and DRAIN pins.
2. The high current path of for this solution is through the MOSFET, therefore it is important to use thick traces for source and drain of the MOSFET to minimize resistive losses.
3. The charge pump capacitor across VCAP and ANODE pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
4. The Gate pin of the SCT53600Q must be connected to the MOSFET gate without using vias. Avoid excessively thin traces to the Gate Drive.
5. Keep the GATE pin close to the MOSFET to avoid increase in MOSFET turn-off delay due to trace resistance.

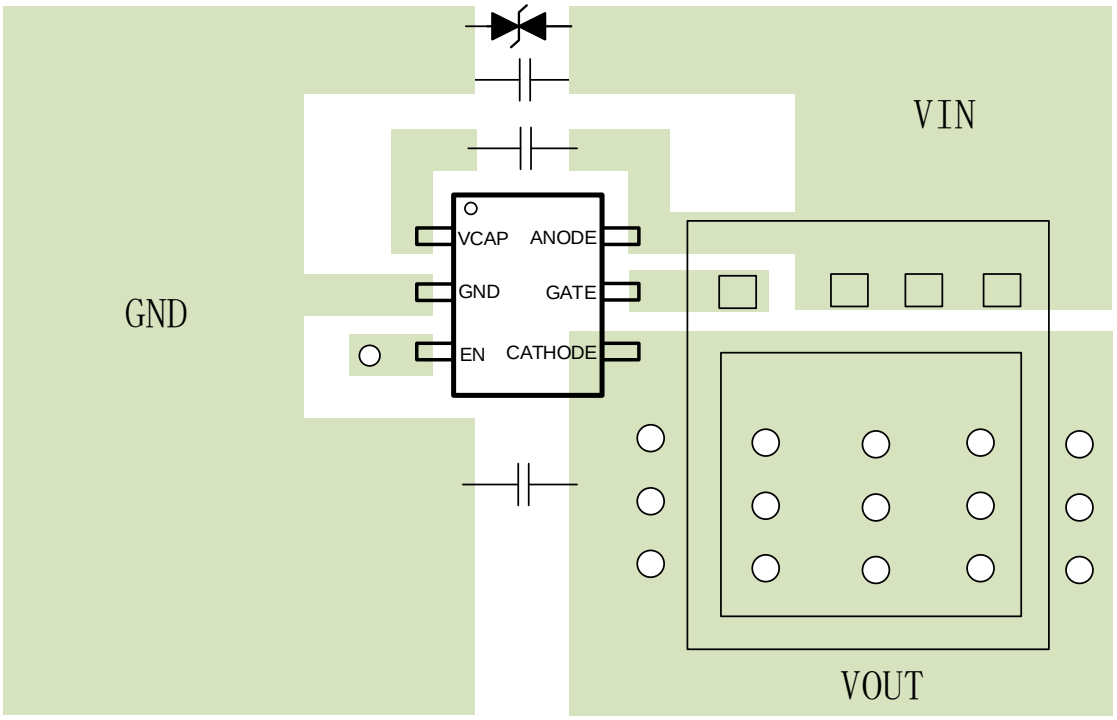
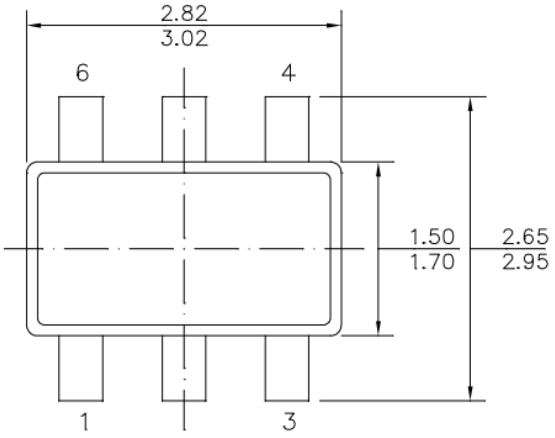
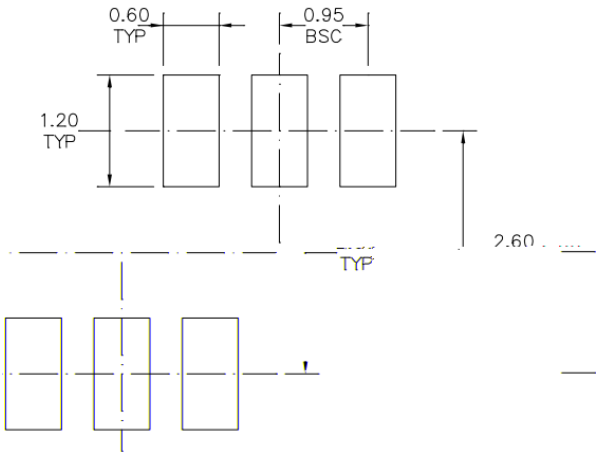


Figure 29. PCB Layout Example

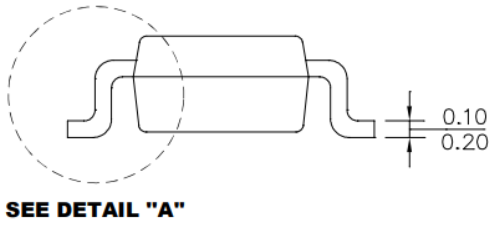
PACKAGE INFORMATION



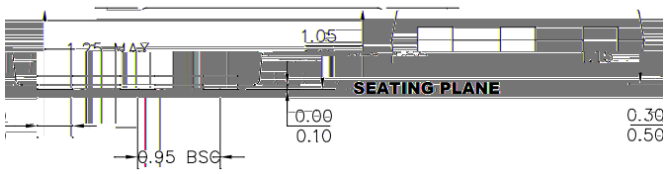
TOP VIEW



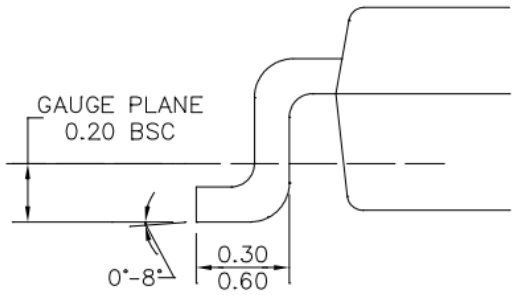
BOTTOM VIEW



SIDE VIEW



FRONT VIEW



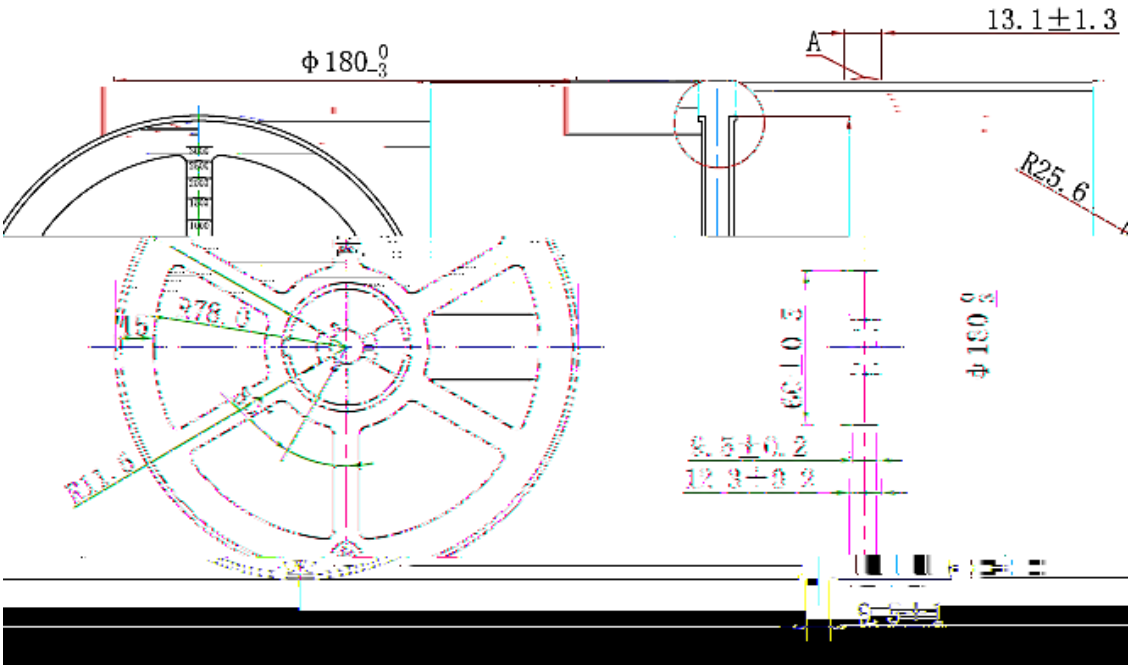
RECOMMENDED LAND PATTERN

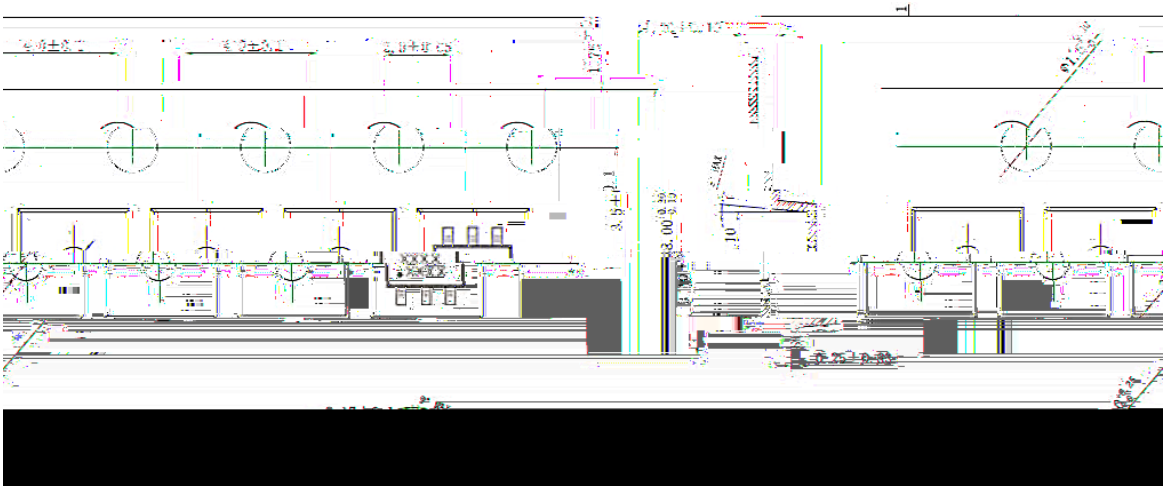
SOT23-6L Package Outline Dimensions

NOTE:

1. THE LEAD SIDE IS WETTABLE.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4. JEDEC REFERENCE IS MO-220.
5. DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION





Feeding Direction

