BST2	8	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	9	Switching node of the half-bridge FETs Q3 and Q4.
SW1	10	Switching node of the half-bridge FETs Q1 and Q2.
BST1	11	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
EN	12	Enable pin. Pull the pin high or keep it floating to enable the IC. When the device is enabled, 5V LDO will start to work if VIN higher than UVLO threshold. After VDD is established, power stage responds to PWM input logic then.
ISNS	13	Current detection output. The voltage of the pin is proportional to the input current.
PWM2	14	PWM logic input to the FET Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q4, and turns on the high-side FET Q3. Logic LOW turns off the high-side FET Q3 and turns on the low-side FET Q4. When PWM input is in the tri-state mode, both Q3 and Q4 are turned off.
PWM1	15	PWM logic input to the FET Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q2, and turns on the high-side FET Q1. Logic LOW turns off the high-side FET Q1 and turns on the low-side FET Q2. When PWM input is in the tri-state mode, both Q1 and Q2 are turned off.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.2	20	V
P_{VIN}	Input voltage range	1	15	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

PARAMETER	THERMAL METRIC	DFN-19L	UNIT
R	Junction to ambient thermal resistance(1)	48	°C/W
R	Junction to case thermal resistance(1)	45	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63140 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63140. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{PVIN1}=V_{PVIN2}=12V, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}	Operating input voltage		4.2		20	V
P_{VIN}	Operating input voltage		1		15	V
V_{IN_UVLO}	V_{IN} UVLO Threshold Hysteresis	V_{IN} rising		3.6 400		V mV
V_{DD_UVLO}	V_{DD} UVLO Threshold Hysteresis	V_{DD} rising		3.8 440		V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V, VIN=12V		1	3	A
I_{SHDN_PVIN}	Shutdown current from PVIN1,PVIN2	EN=0V, PVIN=12V		1	3	uA
I_{VINQ}	Quiescent current from VIN pin	EN floating, VDD=5V, no loading on LDO		300		uA
I_{PVINQ}	Quiescent current from PVIN1, PVIN2	EN floating, VDD=5V, no loading on LDO		50		uA
ENABLE INPUTS and PWM logic						
V_{EN_H}	Enable high threshold			1.18		V
V_{EN_L}	Enable low threshold			1.1		V
V_{IH}	PWM1, PWM2 Logic level high	V3P3=3.3V, VDD=5V	2.65			V
V_{IL}	PWM1, PWM2 Logic level low	V3P3=3.3V, VDD=5V			0.55	V
V_{TS}	PWM1, PWM2 Tri-state voltage		1.2		2	V
Power Stage						
$R_{DSON\_Q1\ Q3}$	High-side MOSFET Q1 Q3 on-resistance	V_{BST1}-V_{SW1}=5V, V_{BST2}-V_{SW2}=5V		16		m
$R_{DSON\_Q2\ Q4}$	Low-side MOSFET Q2 Q4 on-resistance	VDD=5V		16		m
I_{LIM}	High-side current limit threshold			10		A
5V LDO						
V_{DD}	Output voltage	Cout=10uF	4.95	5	5.05	V
I_{DD}	Output current Capability			100		mA
3.3V LDO						
V_{3P3}	Output voltage	Cout=1uF, VDD=5V	3.267	3.3	3.333	V
I_{3P3}	Output current Capability	VDD=5V		100		mA
I_{SC}	Short current			50		mA
Current Sense						
V_{ISNS0}	Voltage with no input current	I_{PGND}=0A ,Tj=25 PWM1=PWM2=0V	0.585	0.6	0.615	V
R_{ISNS}	Input current to output voltage gain	V_{ISNS}=V_{ISNS0}+I_{PGND}*R_{ISNS}	0.98	1	1.02	V/A
V_{ISNS1}	Voltage with 0.6A input current	I_{PVIN}=0.6A, Tj=25	1.176	1.2	1.224	V
V_{ISNS2}	Voltage with 1A input current	I_{PVIN}=1A, Tj=25	1.568	1.6	1.632	V
Protection						
T_{SD}	Thermal shutdown threshold	T_J				

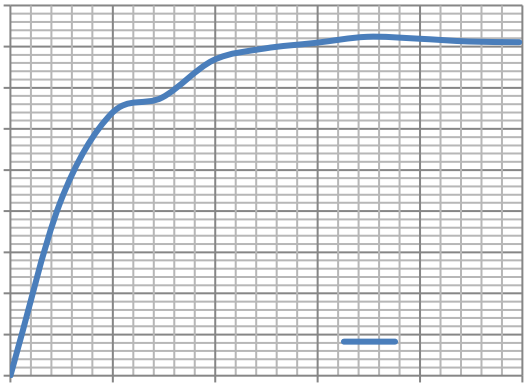


Figure 2. Transfer Efficiency with 5W RX@ Vout=5V

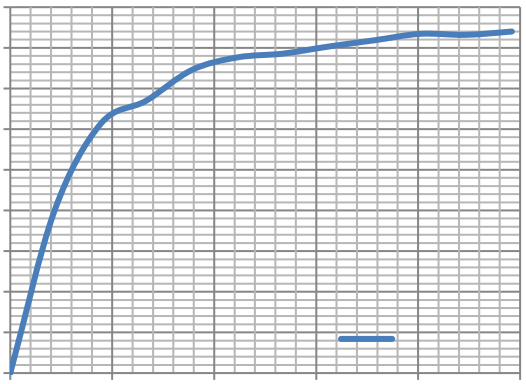


Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

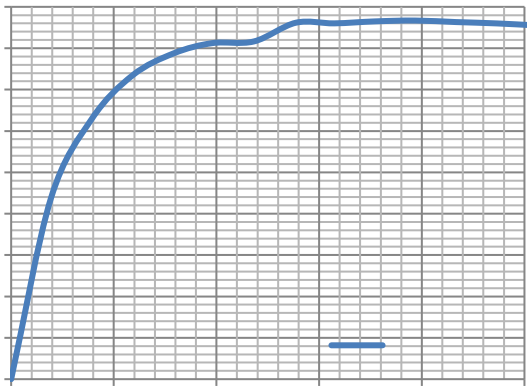


Figure 4. Transfer Efficiency with 15W RX@ Vout=12V

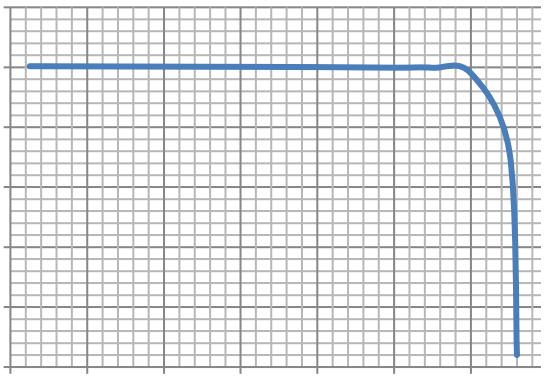


Figure 5. 5V LDO Iout vs Vout

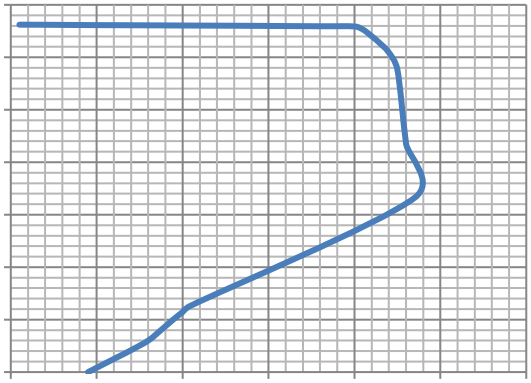


Figure 6. 3.3V LDO Iout vs Vout

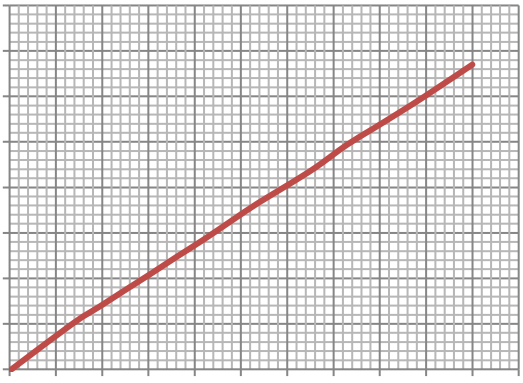


Figure 7. Current Sense Output Voltage vs Iin

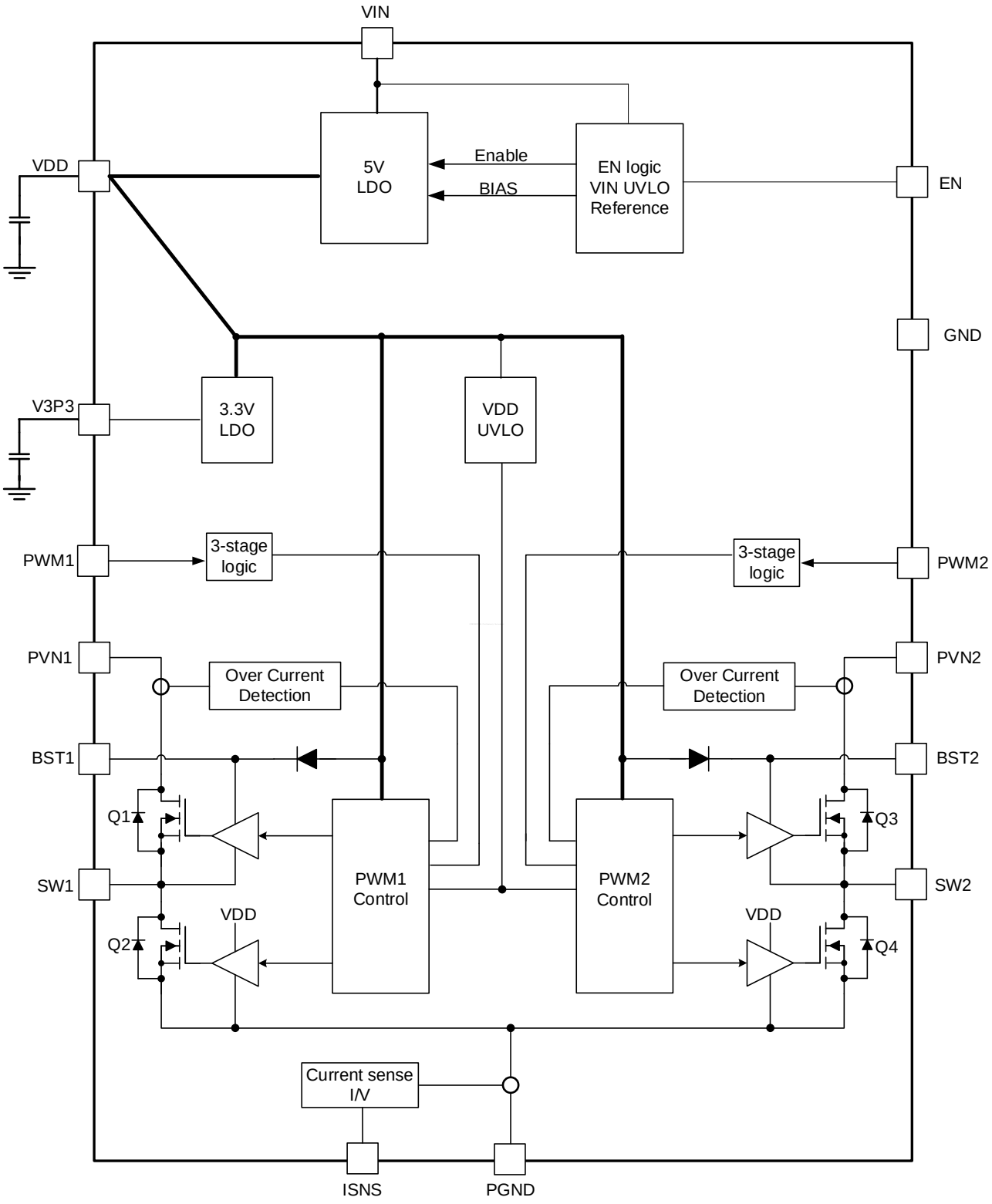


Figure 8. Functional Block Diagram

Overview

The SCT63140 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V output LDO as power supply for external transmitter controller, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU.

The SCT63140 has three power input pins. VIN is connected to the power FETs of 5V LDO. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.2V typically. The maximum operating voltage for PVIN is up to 15V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63140 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort

5V LDO

The SCT63140 has an integrated low-dropout voltage regulator which powered from VIN and supply regulated 5V voltage on VDD pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of external transmitter controller directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VDD pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Full bridge and PWM Control

The SCT63140 integrate full bridge power stage with only 16mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 20KHz to 400KHz for different applications which is completely compatible with WPC's frequency requirement from 100KHz to 205KHz.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

PWM1 and PWM2 also support tri-state input. When PWM input logic first enters tri-state either from logic HIGH or logic LOW, the states of its controlled FETs stay the same. If the PWM input stays in the tri-state for more than 60ns, its controlled FETs are all turned off, and the corresponding SW output becomes high impedance. The FETs stay off until the PWM logic reaches logic HIGH or logic LOW threshold.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

Full Bridge Over Current Protection

The SCT63140 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 10A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 24ms typically.

Current Sense

The SCT63140 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with ±2% accuracy and reports a proportional voltage directly to the ISNS pin. This voltage information on ISNS pin can be send to specialized controller or general MCU for Foreign Object Detection FOD and current demodulation.

When the full bridge of MOSFETs does not work, no current flows to PGND. The DC bias voltage on ISNS pin is 600mV.This DC bias helps set up a suitable voltage bias for the following analog to digital converter in MCU or amplifier for current demodulation. The average input current to voltage conversion gain on ISNS is 1V/A. The equation 3 represent the corresponding relation for the output voltage on ISNS pin and average current to PGND from full bridge.

$$V_{ISNS} = 600mV + I_{PGND} \quad 1V/A \qquad (3)$$

3.3V LDO

The SCT63140 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 1

Typical Application

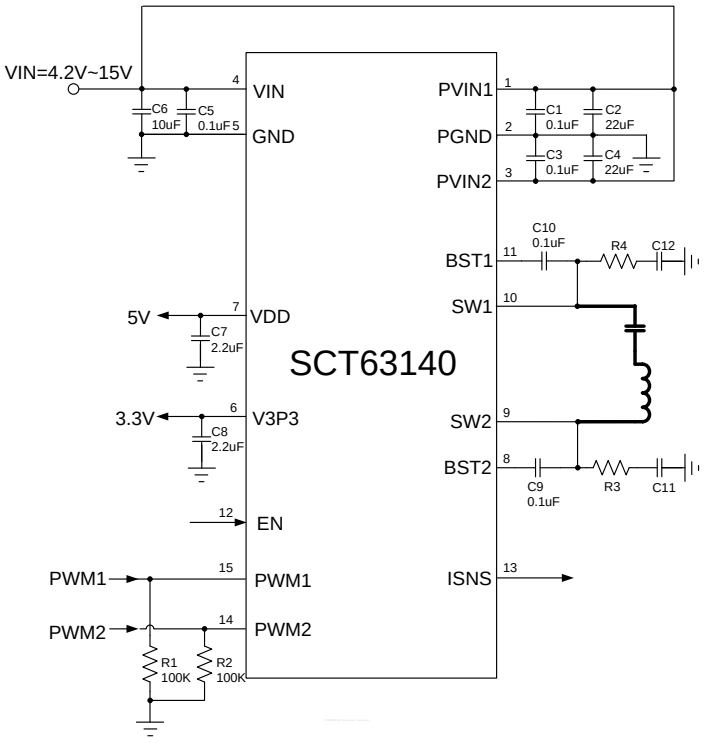


Figure 10. Same Input to VIN and PVIN

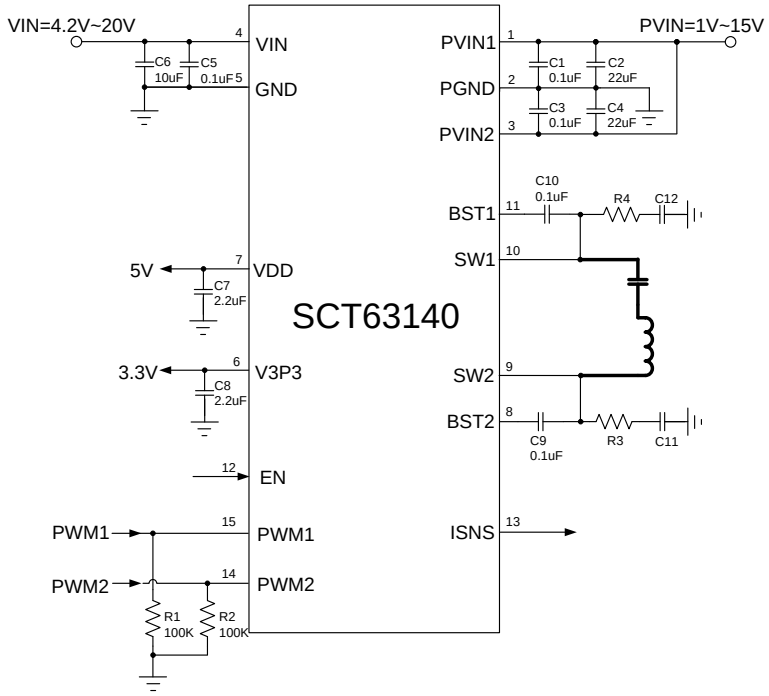


Figure 11. Separate Input to VIN and PVIN

Application Waveforms

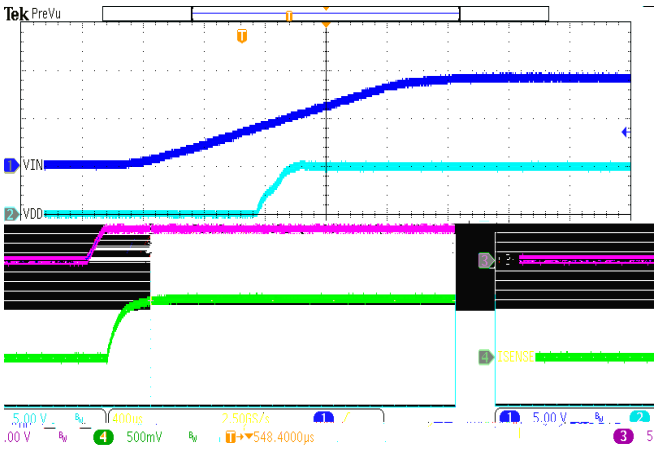


Figure 12. Power Up

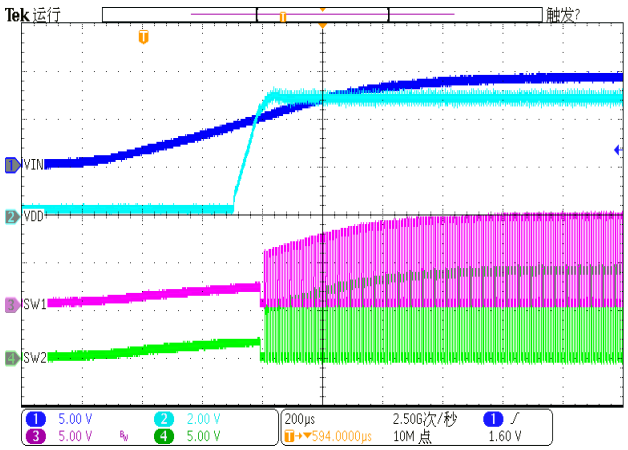


Figure 13. Power Up

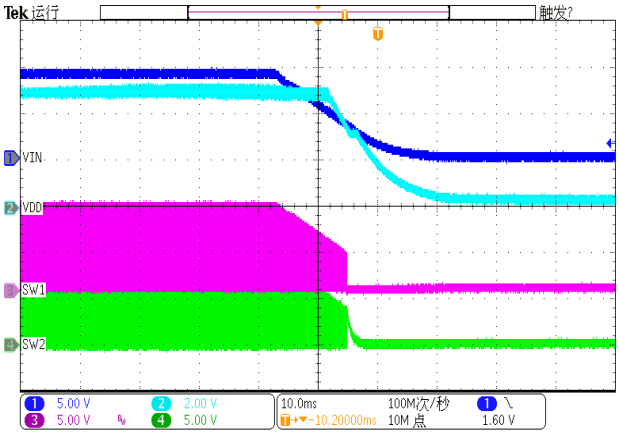


Figure 14. Power Down

Figure 15. Power Down

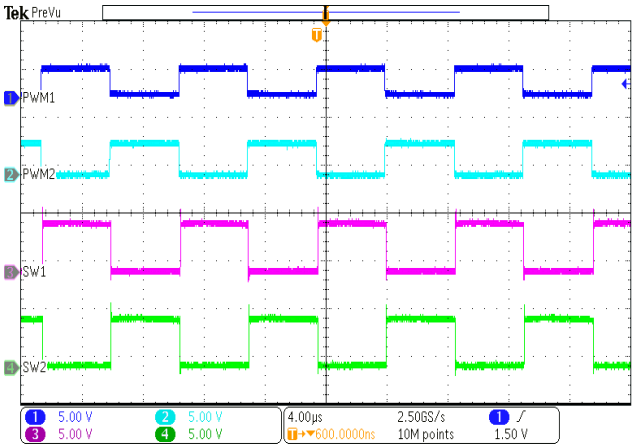


Figure 16. Full bridge @Vin=5V, RX=5W

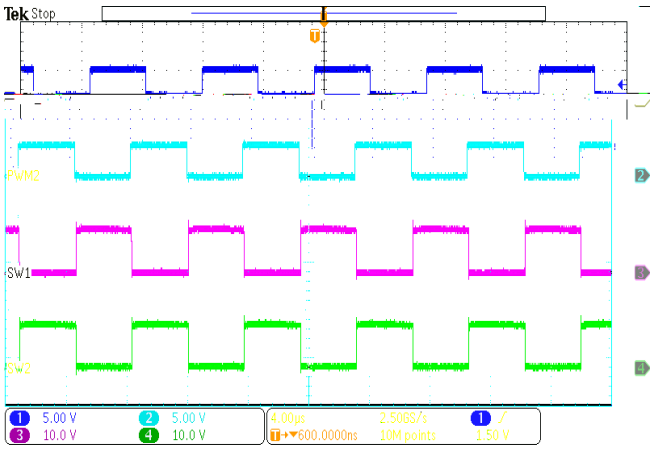


Figure 17. Full bridge @Vin=9V, RX=10W

Layout Guideline

Proper PCB layout is a critical for SCT63140 For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Bypass capacitor for VDD place next to VDD pin.
5. Bypass capacitor for V3V place next to V3V pin.

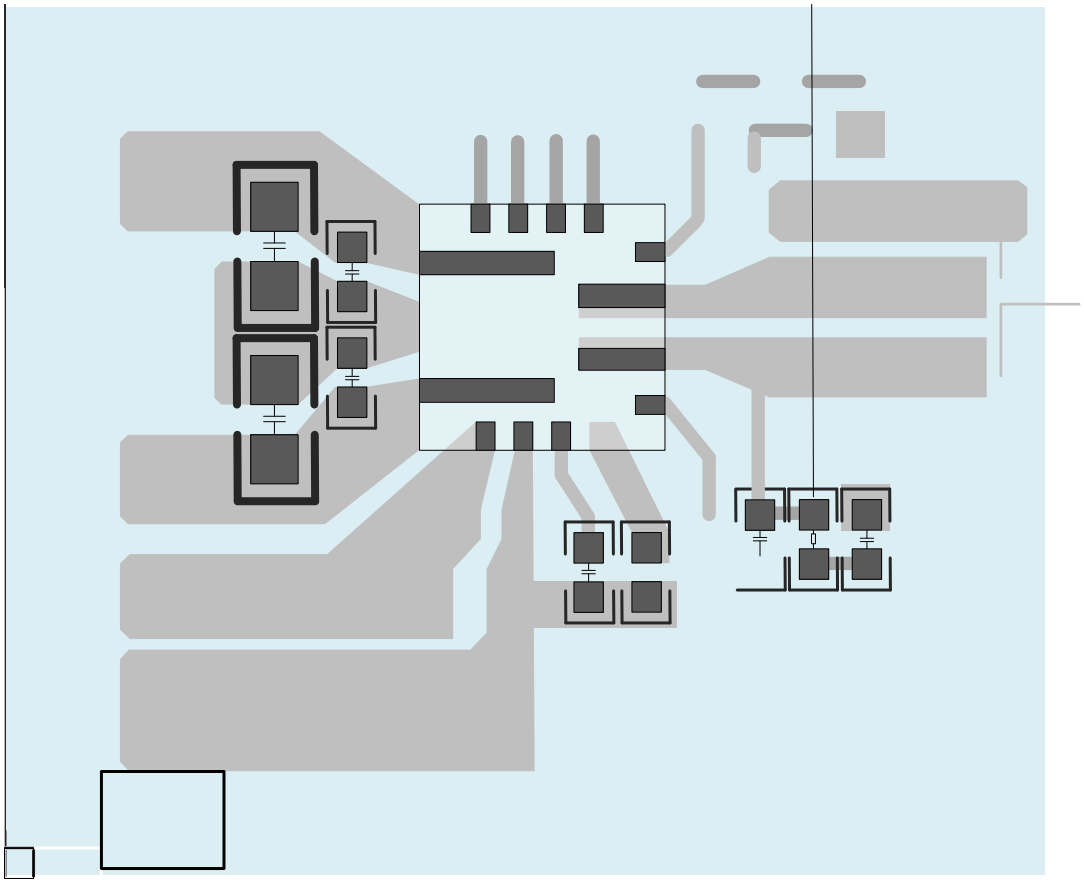
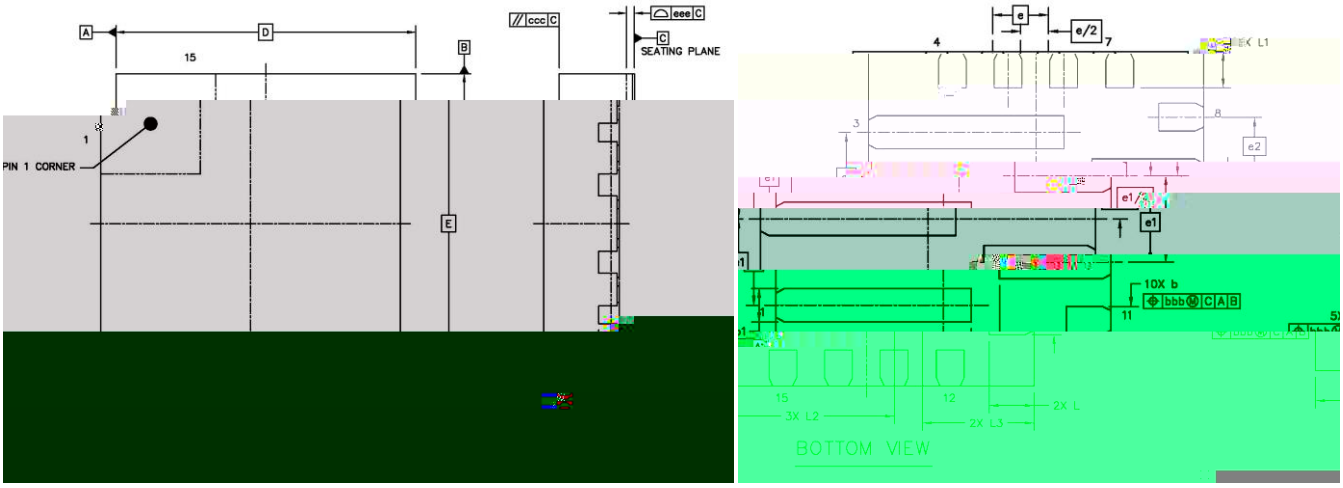


Figure 18. PCB Layout Example

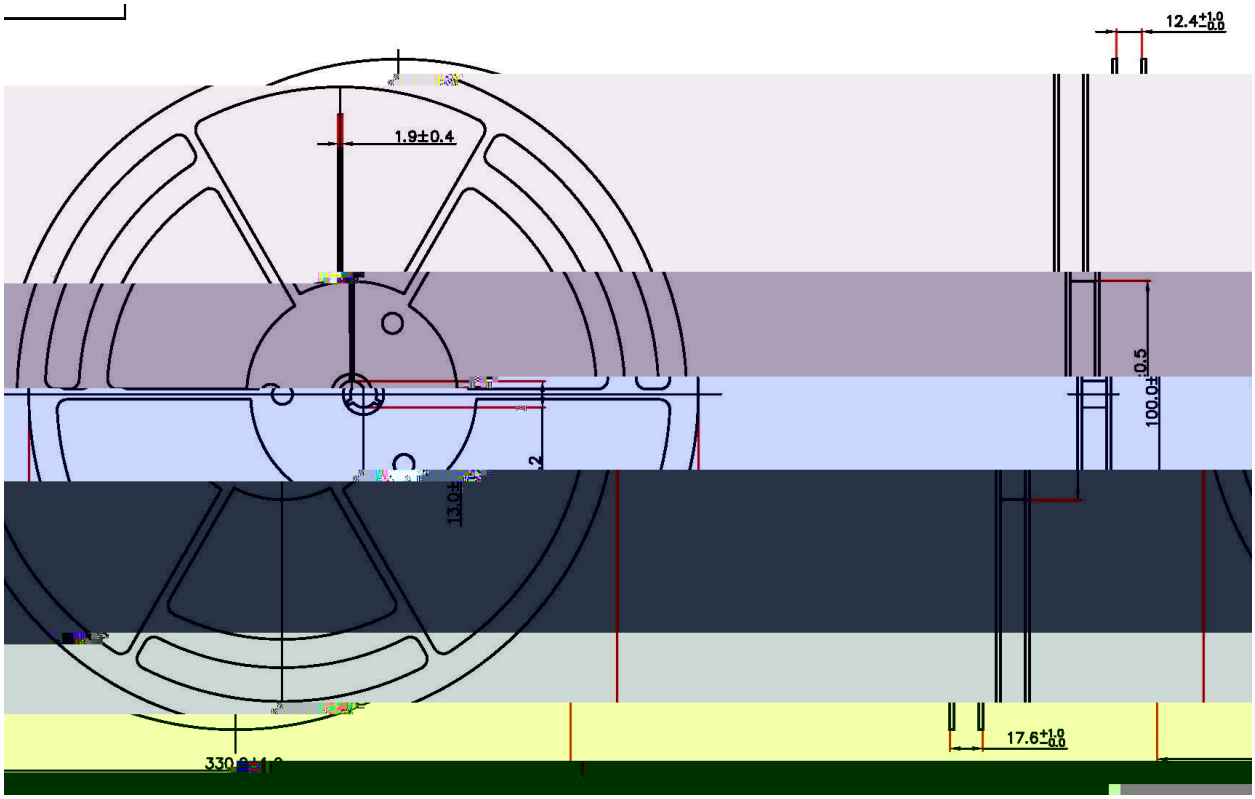


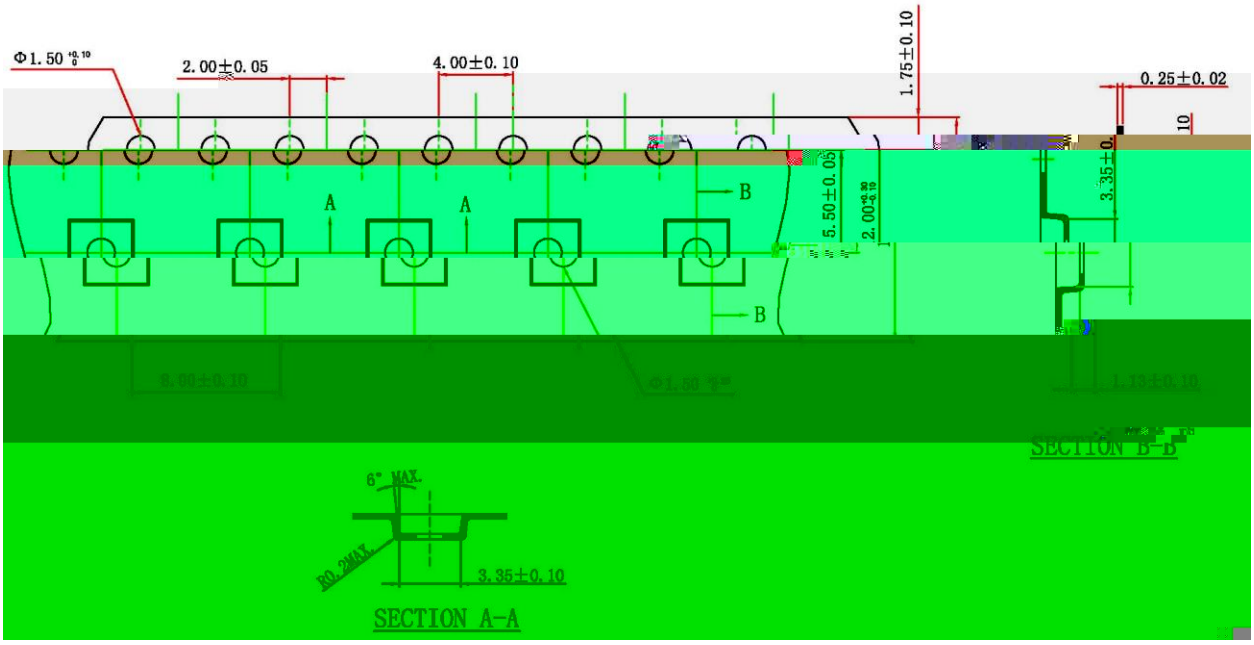
FCQFN-15L (3x3) Package Outline Dimensions

		Symbol	Dimensions in Millimeters		
			Min.	Nom.	Max.
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2		0.55	
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.20	0.25	0.30
		b1	0.25	0.30	0.35
BODY SIZE	X	D		3.00 BSC	
	Y	E		3.00 BSC	
LEAD PITCH		e		0.50 BSC	
		e1		0.775 BSC	
		e2		0.525 BSC	
LEAD LENGTH		L	0.30	0.40	0.50
		L1	0.225	0.325	0.425
		L2	1.65	1.75	1.85
		L3	0.90	1.00	1.10
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.





PN	DESCRIPTION	COMMENTS
SCT63240	20W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter Integrate a 5V-1A Step-down DC/DC converter compared with SC63140.	• VIN Input Voltage Range: 4.2V-20V • PVIN Input Voltage Range: 1V-17V • Up to 20W Power Transfer • Integrated High Efficiency Full-Bridge Power Stage • Integrated High Efficiency 5V-1A Step-down DC/DC Converter • Optimized for EMI • Build in 3.3V-200mA LDO • Provide 2.5V Voltage Reference • Integrated Input Current sense with ±2% accuracy for FOD and modulation • 3.3V and 5V PWM Signal compatible • Input Under-Voltage Lockout • Over current protection • 3mm*4mm QFN-19L Package

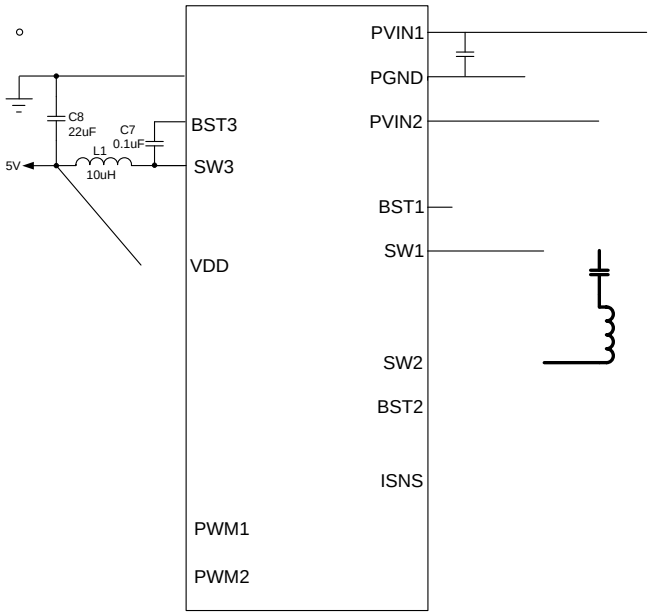


Figure 19. SCT63240 Typical Application

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