- Wide Supply Voltage Range: 4.5V - 24V
- 5.2A Peak Source Current and 6A Peak Sink Current
- Stackable Output for Higher Driving Capability
- Negative Input Voltage Capability: Down to -5V
- TTL Compatible Input Logic Threshold
- Propagation Delay: 12ns
- Typical Rising and Falling Times: 10ns and 6.5ns
- Typical Delay Matching: 1ns
- Low Quiescent Current: 30uA
- Output Low When Input Floating
- Independent Enable Logic for Each Channel
- Available in SOP-8 Package

- IGBT/MOSFET Gate Driver
- Variable Frequency-Drive (VFD)
- Switching Power Supply
- Motor Control
- Solar Power Inverter

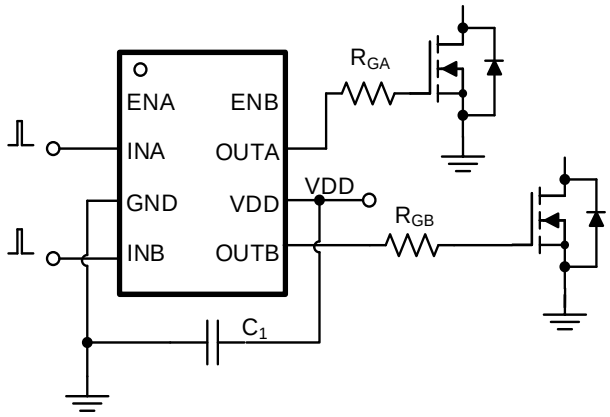
The SCT52250 is a wide supply, dual channel, high speed, low side gate drivers for both power MOSFET and IGBT. Each channel can source and sink 5A peak current along with rail-to-rail output capability. The 24V power supply rail enhances the driver output ringing endurance during the power device transition.

The minimum 12ns input to output propagation delay enables the SCT52250 suitable for high frequency power converter application.

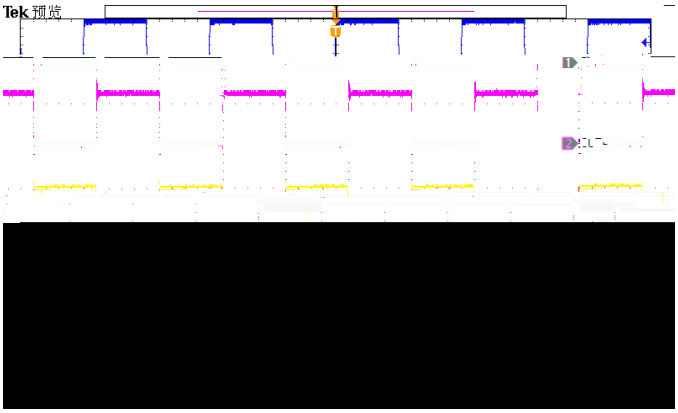
The SCT52250 features wide input hysteresis that is compatible for TTL low voltage logic. The SCT52250 has the capability to handle negative input down to -5V, which increases the input noise immunity.

The SCT52250 has very low quiescent current that reduces the stand-by loss in the power converter. The SCT52250 each channel driver adopts non-overlap driver design to avoid the shoot-through of output stage. The two channels INA and INB have critical propagation delay matching and artificial dead time implemented in output stage, which enable stackable output available when the system needs higher driving capability.

The SCT52250 features 162°C thermal shut down. The SCT52250 is available in SOP-8 package.



SCT52250 Typical Application



Application Waveform

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Production

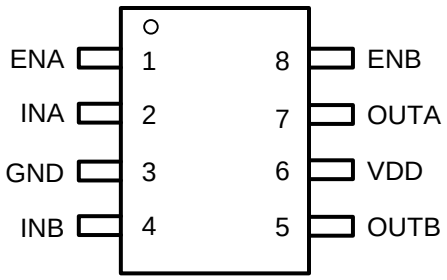
Revision 1.1: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52250STDR	Tape & Reel	4000	2250	8	SOP-8L

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
ENA, ENB	-0.3	26	V
INA, INB	-5	26	V
OUTA, OUTB	-0.3	VDD+0.3	V
OUTA, OUTB (Pulse<0.2us)	-3	VDD+3	V
VDD	-0.3	26	V
Operating junction temperature TJ (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

Top View: SOP-8pin
Plastic



(1) Stresses beyond those listed under Absolut Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

NAME	NO.	PIN FUNCTION
ENA	1	Channel A enable logic input, TTL compatible. Floating logic high.
INA	2	Channel A logic input, TTL compatible. Floating logic low.
GND	3	Power ground. Must be soldered directly to ground plane for thermal performance improvement and electrical contact.
INB	4	Channel B logic input, TTL compatible. Floating logic low.
OUTB	5	Channel B gate driver output
VDD	6	Power Supply, must be locally bypassed by the ceramic cap.
OUTA	7	Channel A gate driver output
ENB	8	Channel B enable logic input, TTL compatible. Floating logic high.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	24	V
$V_{INA,INB}$	Input voltage range	-5	24	
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-0.5	+0.5	kV

(1) HBM and CDM stressing ar1dndeinnddnrnndeLits7-8( )]TJETQ EMC /Span <</MCI10 97/Lang (en-US)>BDC q0.00000912 0 612 792 reW*nBT/F

V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO	V_{DD} rising		4.2	4.5	V
	Hysteresis			320		mV
I_Q	Supply current	EN=V_{DD}=3.5V, INA=INB=GND		30		uA
		EN=V_{DD}=12V, INA=INB=GND		126		uA
INPUTS						
V_{INA,INB_H}	Input logic high threshold			2.15	2.4	V
V_{INA,INB_L}	Input logic low threshold		0.8	1.1		V
V_{IN_Hys}	Hysteresis			1.05		V
V_{ENA,ENB_H}	Enable logic high threshold			2.15	2.4	V
V_{ENA,ENB_L}	Enable logic low threshold		1.1	1.25	1.3	V
V_{EN_Hys}	Hysteresis			0.9		V
OUTPUTS						
I_{SRC}	Output source peak current(1)	C_{Load}=0.22uF, F_{SW}=1kHz		5.2		A
I_{SINK}	Output sink peak current(1)	C_{Load}=0.22uF, F_{SW}=1kHz		6		A
V_{DD_VOH}	Output output high voltage	I_{OUT}= - 10mA		50	80	mV
V_{OL}	Output low voltage	I_{OUT}= 10mA		4.35	8	mV
R_{OH}	Output pull high resistance (only PMOS ON)	I_{OUT}= - 10mA	3	5	8	
R_{OL}	Output pull low resistance	I_{OUT}= 10mA	0.3	0.435	0.8	
Timing						
T_R	Output rising time	C_{Load}=1.8nF		10		ns
T_F	Output falling time	C_{Load}=1.8nF		6.5		ns
T_{D_IN}	Input to output propagation delay, Rising edge			12		ns
	Input to output propagation delay, Falling edge			12		ns
T_{M_IN}	Input to output delay matching			1		ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		20		ns
Protection						
T_{SD}	Thermal shutdown threshold	T_J rising		162		°C
	Hysteresis			25		°C

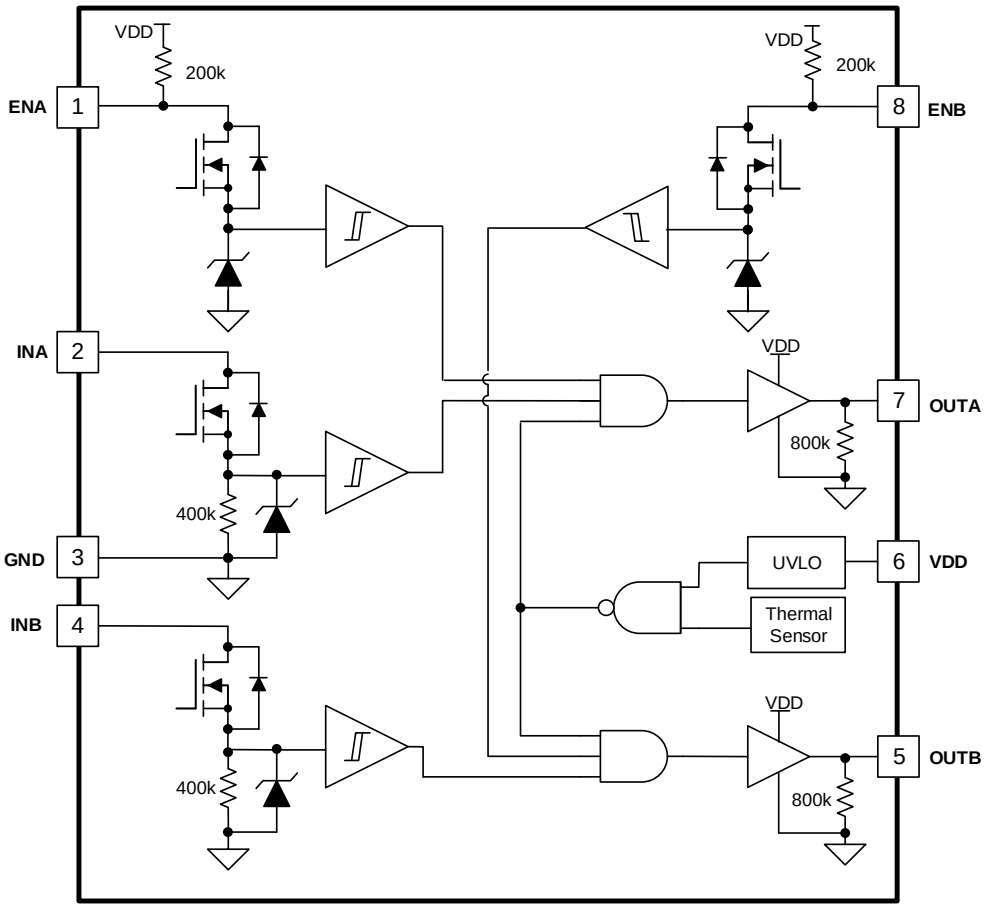
(1)Guaranteed by design

V_{IN}=12V, T_A= 25°C.

Figure 1. UVLO vs Temperature

Figure 2. Supply current vs Temperature

Figure 3.



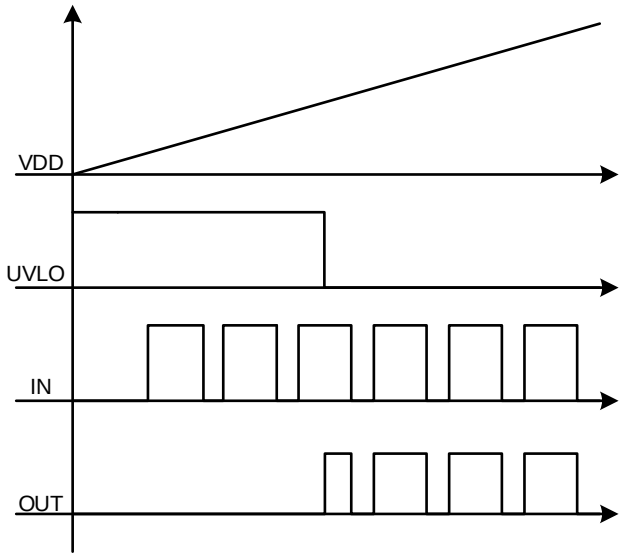
Overview

The SCT52250 is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 5A peak current along with the minimum propagation delay 12ns from input to output. The 1ns delay matching and the stackable output characteristics support higher driving capability demanding in high power converter application. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output improves the SCT52250 output stage robustness during switching load fast transition. The SCT52250 has flexible input and enable pin configuration, table 1 shows the device output logic truth table.

. Table 1: the SCT52250 Device Logic.

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	Floating	Floating	L	L
Floating	Floating	L	L	L	L
Floating	Floating	L	H	L	H
Floating	Floating	H	L	H	L
Floating	Floating	H	H	H	H

VDD Power Supply



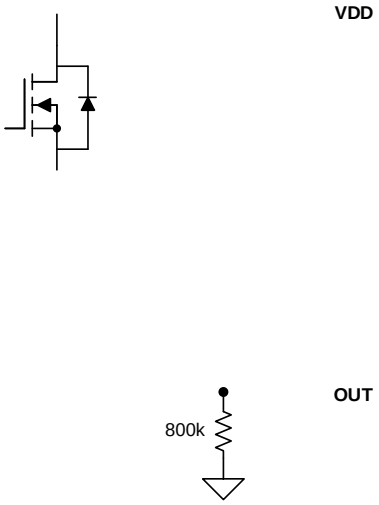


Figure 12. SCT52250 Output Stage

Stackable Output

The SCT52250 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. For example, in a Boost Power Factor Correction converter, there are 2 power MOSFET in parallel to support higher power output capability. The two power MOSFET are preferred to be driven by a common gate control signal. By using SCT52250, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA and INB. As a result, a single input signal controls the stacked output combination. To support the stackable output, each channel output stage artificially implements up to 5ns dead-time to avoid the possible shoot-through between two channels as shown Figure 13.

Due to the rising and falling threshold mismatch between INA and INB, cautions must be taken when implementing stackable output of OUTA and OUTB together. The maximum mismatch between INA and INB input threshold is up to 10mV (maximum cross temperature), as a result the allowed minimum slew rate of input logic signal is 2V/us. The following suggestions are recommended when INA and INB connected together and along with the OUTA and OUTB:

1. Apply the fast slew rate dv/dt on input (2 V/us or greater) to avoid

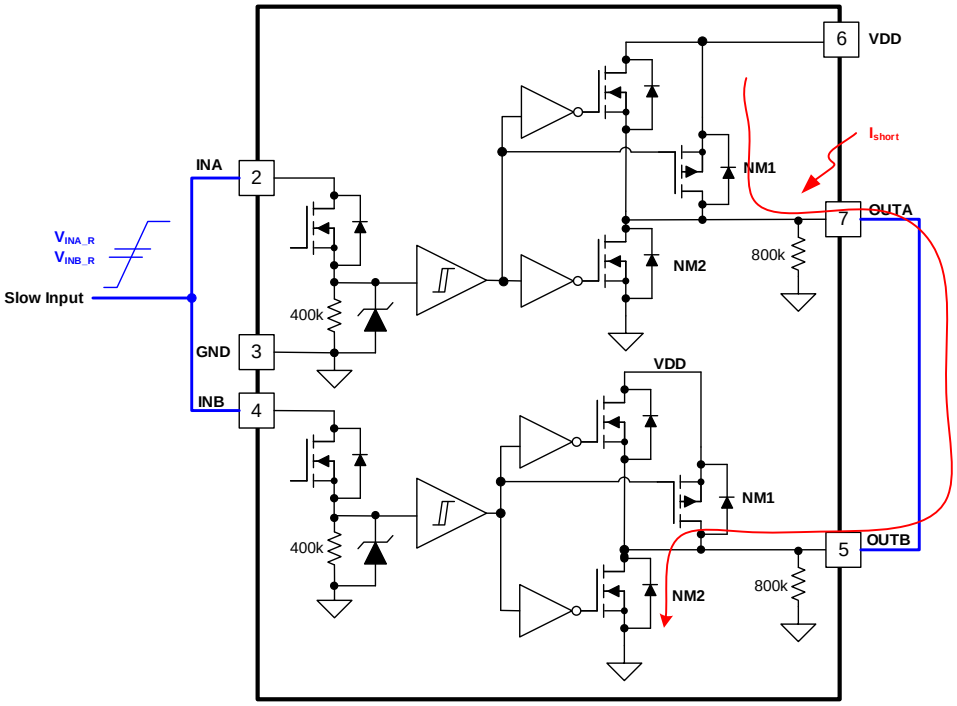


Figure 13. SCT52250 Stackable output

The Figure 14 and Figure 15 shows the stackable output with 2V/us input signal.

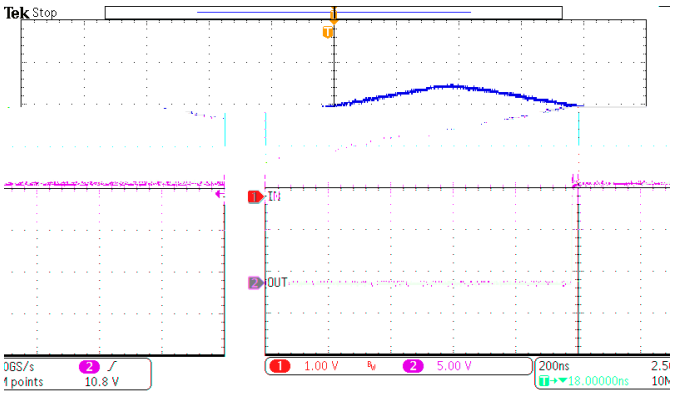


Figure 14. Driver Switching ON

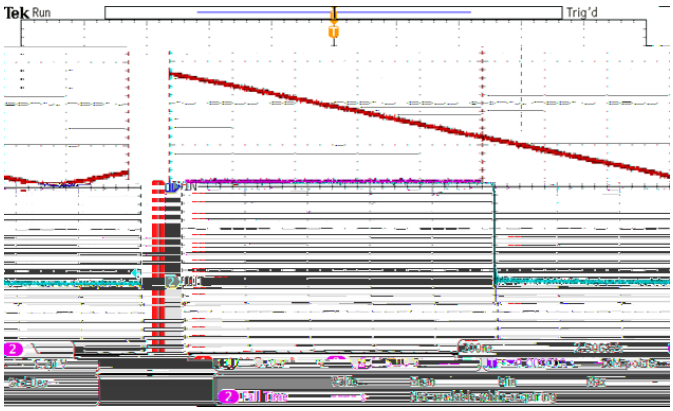


Figure 15. Driver Switching OFF

Thermal Shutdown

Once the junction temperature in the SCT52250 exceeds 162° C, the thermal sensing circuit stops switching until the junction temperature falling below 137° C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

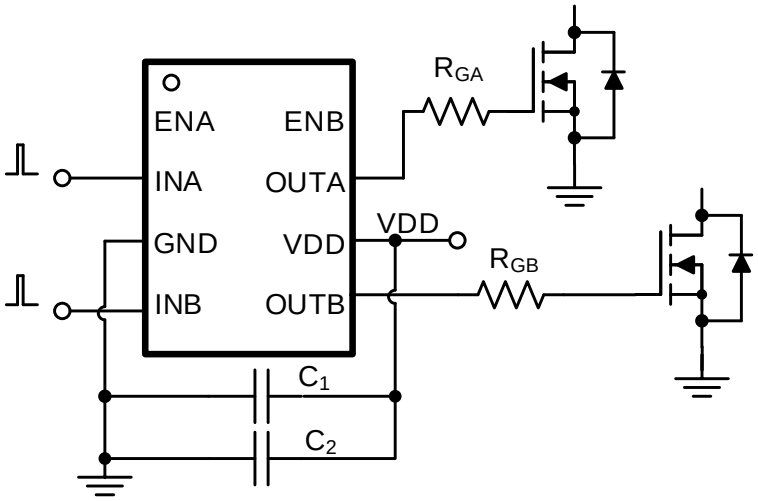


Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52250 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52250 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52250 is:

(1)

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52250 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

(2)

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

(3)

Where

- R_{OH} is the equivalent pull up resistance of SCT52250
- R_{OL} is the pull down resistance of SCT52250
- R_G is the gate resistance between driver output and gate of power device.

Application Waveforms

VDD=12V unless otherwise noted

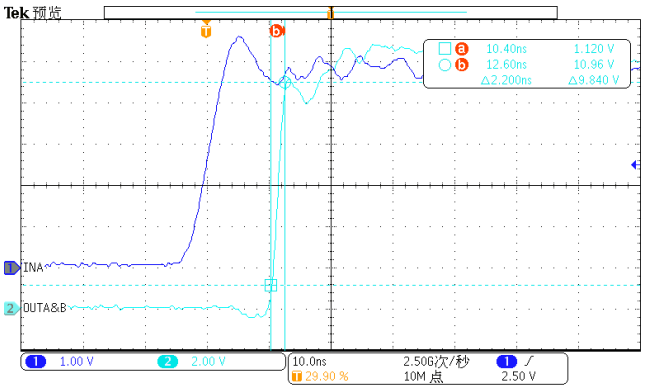


Figure 17. Driver Switching ON (Out capacitance=0nF)

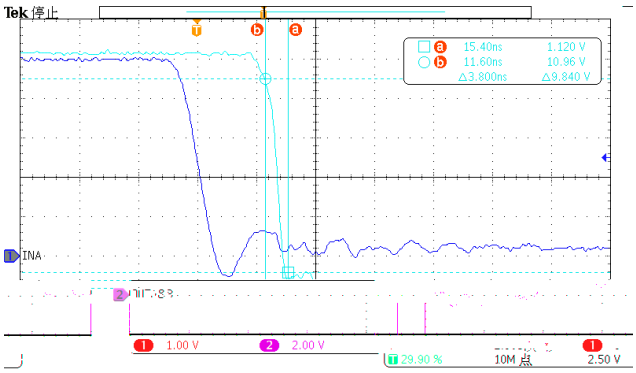


Figure 18. Driver Switching OFF (Out capacitance=0nF)

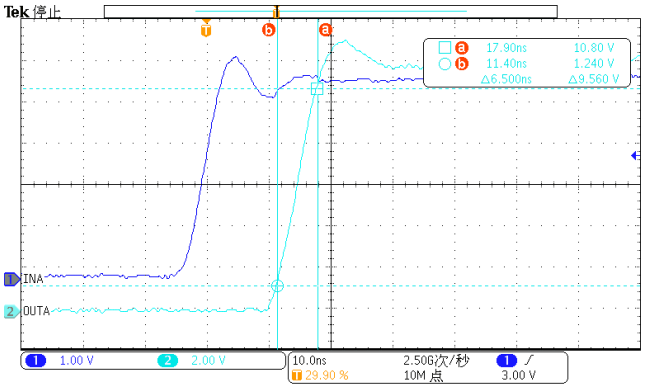


Figure 19. Driver Switching ON (Out capacitance=1.8nF)

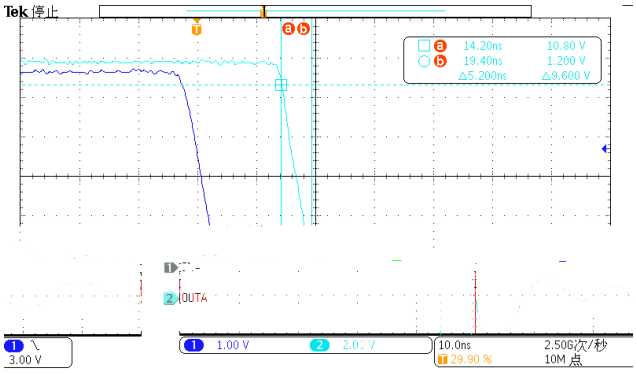


Figure 20. Driver Switching OFF (Out capacitance=1.8nF)

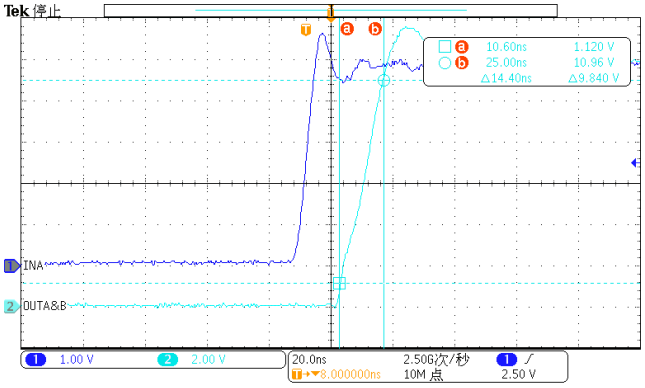


Figure 21. Driver Switching ON (Out capacitance=3.3nF)

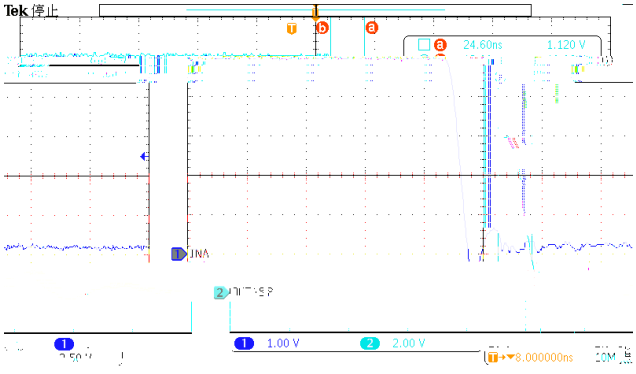


Figure 22. Driver Switching OFF (Out capacitance=3.3nF)

Application Waveforms
VDD=12V unless otherwise noted

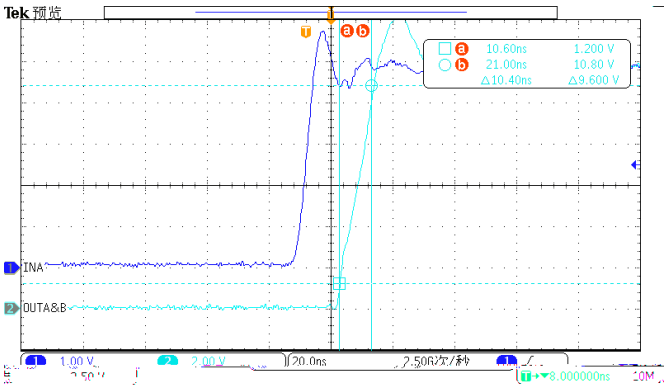


Figure 23. Stackable Output Rise (Out capacitance=3.3nF)

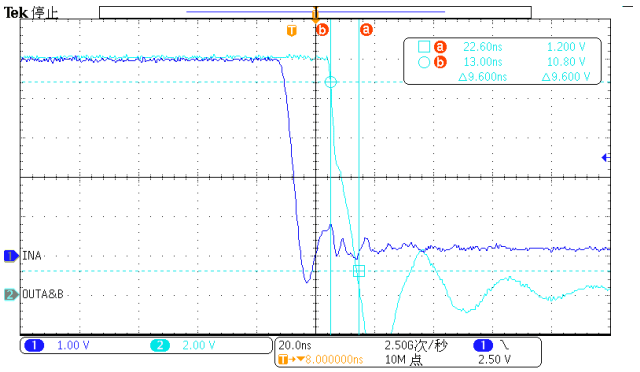


Figure 24. Stackable Output Fail (Out capacitance=3.3nF)

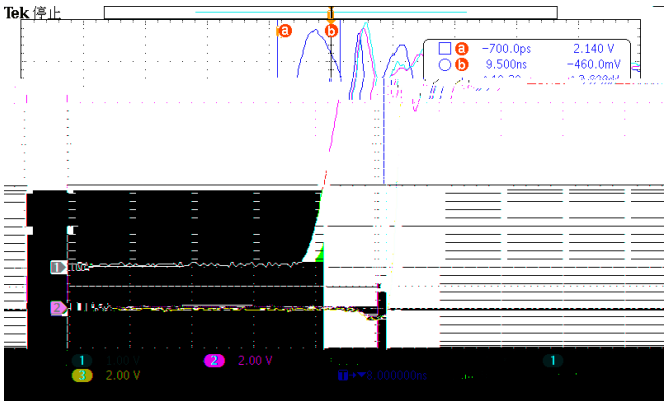


Figure 25. Delay Matching Rise (Out capacitance=1.8nF)

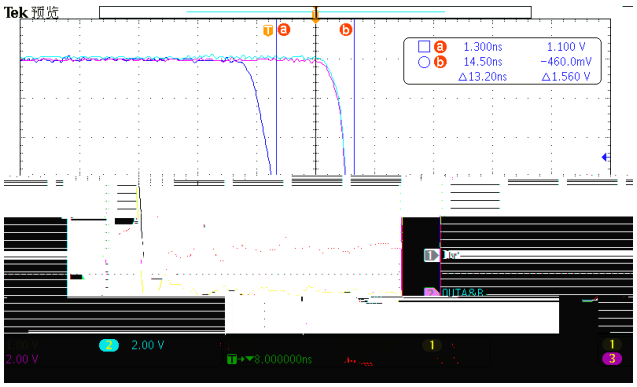


Figure 26. Delay Matching Fail (Out capacitance=1.8nF)

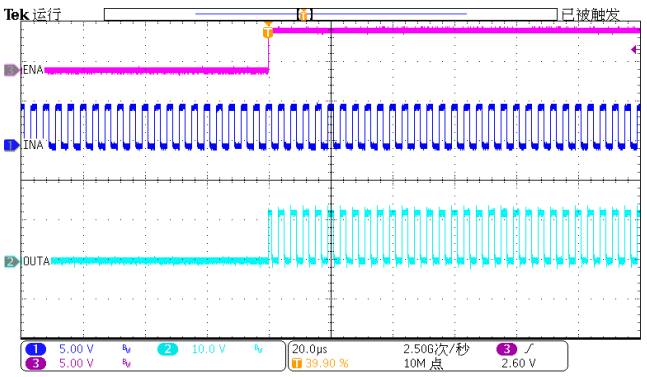


Figure 27. Enable

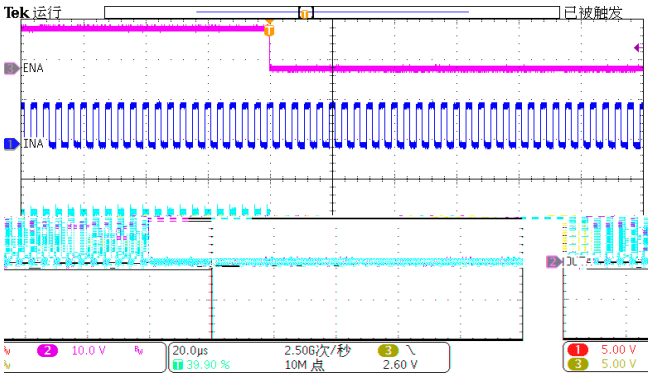
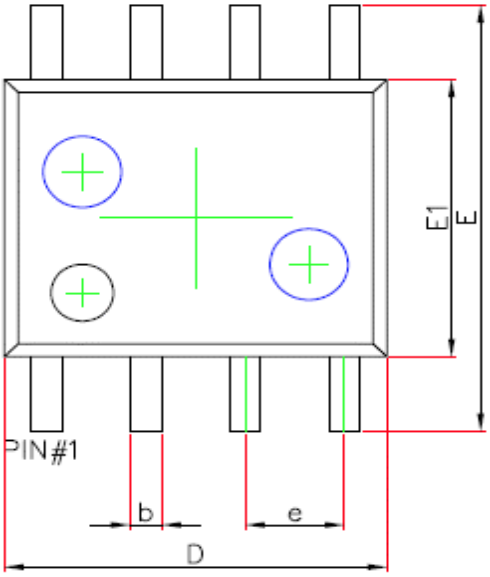


Figure 28. Disable

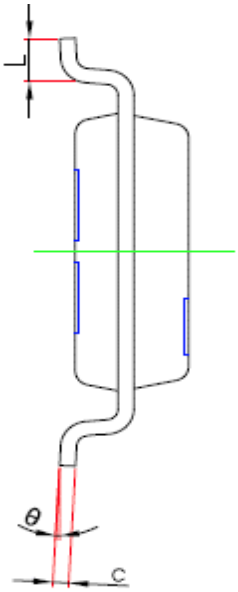
Layout Guideline

The SCT52250 provides the 5A output driving current and features very short rdt12 0 612 3 and fall 3 ti12 0me at the power devices gate. The high di/dt causes driver output unexpecteding when the driver output loop dt12 0 not designed wel12 0le re3ulator couldt12 0uffer from malfunction and EMI dt12 0e dproblems the power device dgate dhas t12 0erdous rd 3 6-6(3)]TJETQ EMC /Span <</MCID 11/Lang (en-US)>BDC q0.00000912 0 612 792 reW* nBT/F2 9.96 Tf1 0 0 1 83.904 Spa

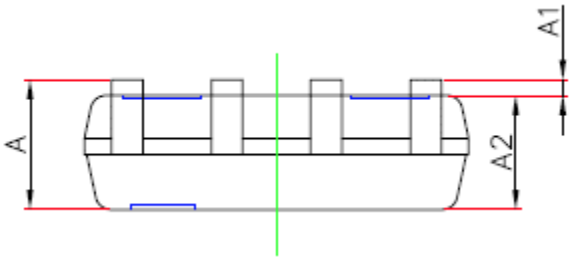
Put the SCT52250 as clas post12 0 612ble to the power device to minimize the gate driving lp 6-6(c)-3(l) 0uding the driver output and power devdce gate. The power pl decoupl 6-6(3)]TJETQ EMC /Span <</MCID 23/Lang (en-US)>BDC q0.00000912



TOP VIEW



BOTTOM VIEW

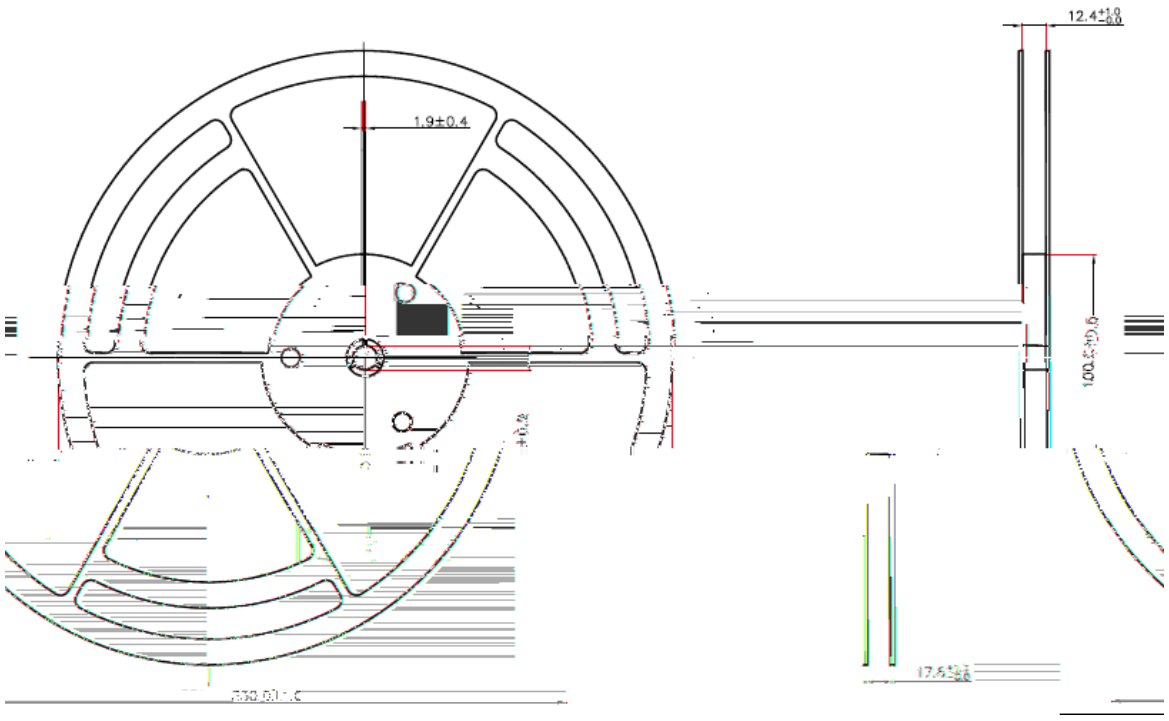


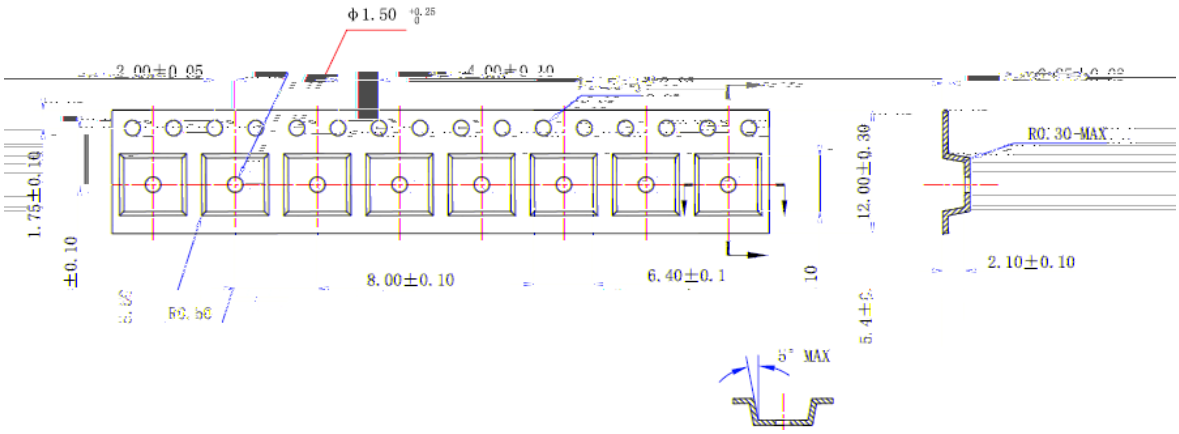
SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1	3.8		4.0
e	1.27BSC		
L	0.4		1.27
	0°		8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.





Feeding Direction

