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- Wide Input Voltage Range: 2.7V-12V
- Wide Output Voltage Range: 4.5V-12.6V
- Fully Integrated 17
  14
- Up to 93% Efficiency at Vin=3.3V, Vout=9V, and Iout=2A
- Programmable and Up to 9.5A Peak Switch Current Limit
- Typical Shut-down Current: 1uA
- Quiescent Current: 150uA
- Adjustable Switching Frequency: 200KHz to 2.2MHz
- PFM Operation Mode at Light Load
- Internal Soft Start and External Compensation
- Cycle-by-Cycle Overcurrent Protection
- Output Overvoltage Protection
- Thermal Shutdown Protection: 160°C
- QFN-11 2mm x 2.5mm Package

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- Bluetooth Speaker
- Portable POS Terminal
- Quick Charge Power Bank
- E-Cigarette
- Outdoor Flashlight

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The SCT1271 is a high efficiency synchronous boost converter with fully integrated a 17 high-side MOSFET and a 14 low-side MOSFET, featuring 2.7V to 12V input voltage range to support single cell or two cell Lithium ion/polymer batteries and up to 9.5A peak switch current. The switch current limit can be adjustable with an external resistor. The SCT1271 has 7A continuous switch current capability and provides output voltage up to 12.6V.

The SCT1271 adopts constant off-time peak current control to provide fast transient response. An external compensation network allows flexibility setting loop dynamics to achieve optimal transient performance at different load conditions.

The SCT1271 works in the PWM at moderate and heavy load condition. The SCT1271 offers PFM mode at light load condition. The switching frequency is adjustable from 200KHz to 2.2MHz.

The SCT1271 features output overvoltage protection and thermal shutdown protection when the device over loads.

The device is available in a QFN-11 2mm x 2.5mm package.

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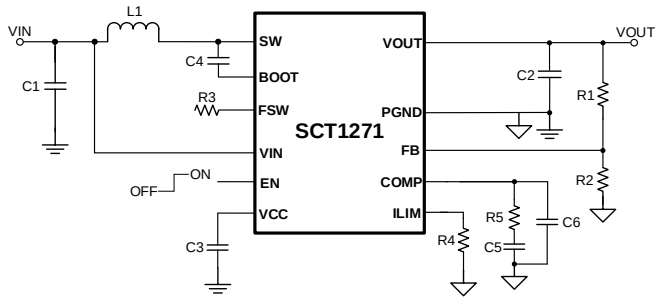
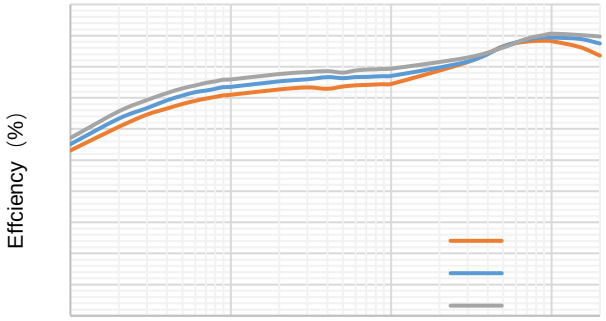




Efficiency vs Load Current, Vout=9V

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update T_J to 150 ºC

Revision 1.2: Update Equation 3

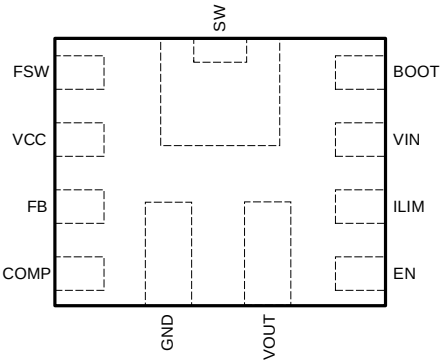
PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT1271FQA	1271	11-Lead 2mm×2.5mm Plastic QFN

1）For Tape & Reel, Add Suffix R (e.g. SCT1271FQAR)

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	21.5	V
VIN, SW, FSW, VOUT	-0.3	14.5	V
VCC, LIM, FB, EN, COMP, MODE	-0.3	5.5	V
BOOT-SW	-0.3	5.5	V
Operating ambient temperature T_A	-40	125	°C
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

Top View: 11-Lead Plastic QFN 2mm x 2.5mm



(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

ILIM	8	Inductor peak current limit set point input. A resistor connecting this pin to ground sets current limit through low-side power FET.
VIN	9	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
BOOT	10	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
SW	11	Switching node of the boost converter.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	12	V
V_{OUT}	Output voltage range	4.5	12.6	V
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	QFN-11L	UNIT
R	Junction to ambient thermal resistance(1)	53.4	°C/W
R	Junction to case thermal resistance(1)	59.2	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT1271 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT1271. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		12	V
V_{OUT}	Output voltage range		4.5		12.6	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.5 200		V mV
I_{SD}	Shutdown current	EN=0, no load and measured on VIN pin		1		uA
I_Q	Quiescent current from VIN	EN=2V, no load, no switching		1.8		uA
	Quiescent current from VOUT			150		uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.75		V
V_{CC_UVLO}	VCC UVLO threshold	V_{IN} falling		2.2		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB		0.98	1	1.02	V
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		200		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		24		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		24		uA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V, R_{ILIM}=100		2.2		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.2V, R_{ILIM}=100 , PFM		0.9		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			17		
R_{DSON_L}	Low side FET on-resistance			14		
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}=100	7.2	8	8.8	A
		R_{ILIM}=84		9.5		A
Enable						
V_{EN}	Enable high threshold Enable low threshold		 0.4		1.2	V V
R_{EN}	Enable pull down resistance			750		
T_{SS}	Soft-start Current			4		ms
Switching Frequency						
F_{SW}	Switching frequency	R_{FSW} $_{OUT}$=12V		500		kHz
t_{ON_MIN}	Minimum on-time	R_{FSW} $_{OUT}$=12V		170		ns
Protection						

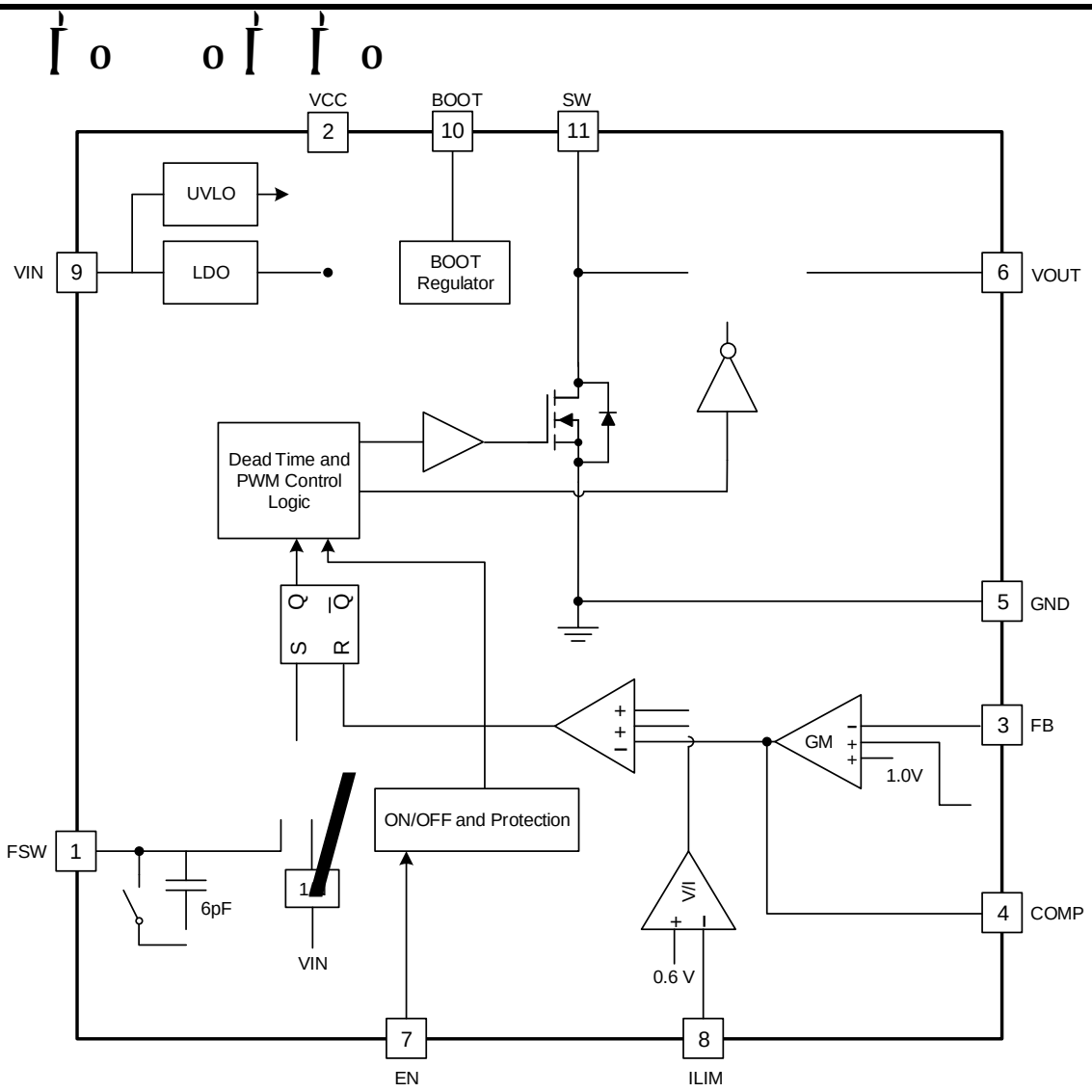


Figure 7. Functional Block Diagram

Overview

The SCT1271 device is a fully integrated synchronous boost converter, which regulates output voltage higher than input voltage. The constant off-time peak current mode control provides fast transient with pseudo fixed switching frequency. When low-side MOSFET Q1 turns on, input voltage forces the inductor current rise. Sensed voltage on low-side MOSFET peak current rises above the voltage determined by COMP. After the inductor current reachode

(minimum 0.4V). An internal 75 the ground. Floating EN pin automatically disables the device.

The SCT1271 features fixed 4ms soft start to prevent inrush current during power-up.

Adjustable Peak Current Limit

The SCT1271 boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 1 or Figure 5 to calculate the peak current limit.

$$( ) = \frac{800}{( )} \quad (1)$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance between ILIM pin to ground.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, the SCT1271 will enter hiccup mode to protect the low-side MOSFET Q1 and the body diode of the high-side MOSFET Q2 from damage even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Adjustable Switching Frequency

The SCT1271 features a wide adjustable switching frequency ranging from 200kHz to 2.2MHz. The switching frequency is set by a resistor connected between the FSW pin and the GND pin of SCT1271. Do not leave the FSW pin open. Use Equation 2 to calculate the resistor value required for a desired frequency.

$$= \frac{\frac{1}{-70} - \quad \_\_\_\_}{} \quad (2)$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 70 ns
- C_{FREQ} = 6 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Over Voltage Protection and Minimum On-time

The SCT1271 features VOUT pin over voltage protection. If the VOUT pin is above 13.2V typical, the device stops switching immediately until the VOUT pin drops below 12.92V. The OVP function prevents the connected output circuitry from un-predictive overvoltage.

The low-side MOSFET has minimum on-time 170ns typical limitation. While the device is operating at minimum on time and further increasing Vin push output voltage beyond regulation point. With output and feedback over voltage protection, the converter skips pulse with turning off high-side MOSFET and prevents output running higher to damage the load.

PFM Mode

The SCT1271 improves the efficiency at light load with the PFM mode. When the converter operates in light load MO 0 2(S)4(F)341 445.9 0 612 7* n0(2)]TJETQq4o0.480 g(l)5(o)*qTJ3[46000912 0 52 7reW* nB0 g396 Tf1o off high

and reaches a threshold with respect to the peak current of I_{LIM} / 10, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the SCT1271 delivers, the output voltage increases above the nominal setting output voltage. The SCT1271 extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 1.0% higher than the nominal setting voltage. With the PFM operation mode, the SCT1271 keeps the efficiency above 70% even when the load current decreases to 1 mA. At light load, the output voltage ripple is much smaller due to low peak inductor current. Refer to Figure 17.

Thermal Shutdown

Once the junction temperature in the SCT1271 exceeds 164 C, the thermal sensing circuit stops switching until the junction temperature falling below 140 C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

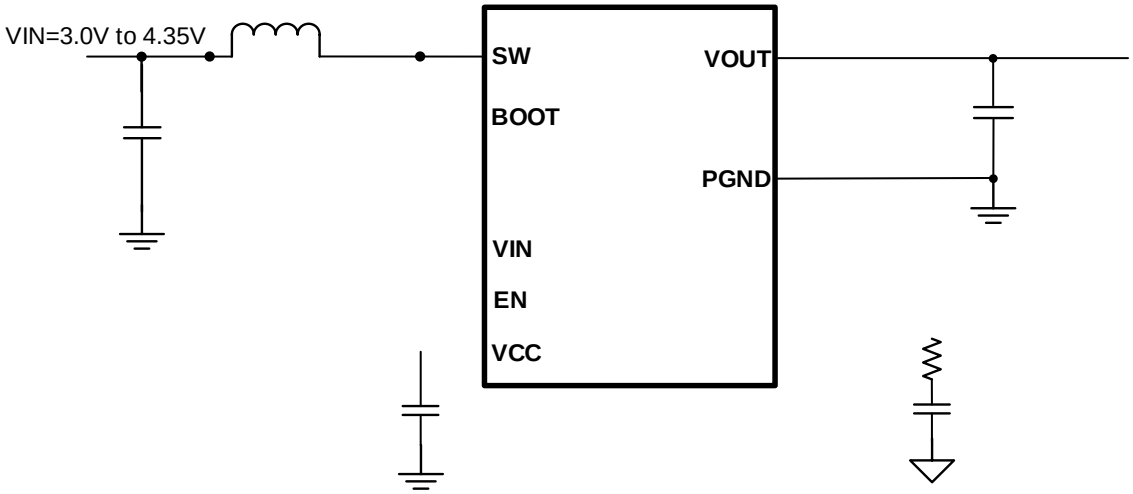


Figure 8. One Cell Battery Input, 9V/2A (20W) Output

Design Parameters

Design Parameters	Example Value
Input Voltaget Voltage	

Switching Frequency

The resistor connected from FSW to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 3. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

$$= \frac{\frac{1}{+70} - \quad \_\_\_}{\quad} \qquad (3)$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 70 ns
- C_{FREQ} = 6 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Table 1. R_{FSW} Value for Common Switching Frequencies (Vin=3.6V, Vout=9V, Room Temperature)

Fsw	R_{FREQ}
200 KHz	590
370 KHz	350
560 KHz	235
860 KHz	150
1000 KHz	126
2000 KHz	51

Peak Current Limit

Using the correct external resistor at ILIM pin sets the peak input current. Table 2 shows the resistor value for inductor peak current limit. For a typical current limit of 9.5A, the resistor value is 84 . The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage.

$$(\ ) = \frac{800}{(\ \ )} \qquad (4)$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance of ILIM pin to ground

Table 2. R_{LIM} Value for Inductor Peak Current (Vin=3.6V, Vout=9V, L=2.2uH, Room Temperature)

I_{LIM}	R_{LIM}
9.5 A	
8 A	100
5.6A	
4A	

Output Voltage

The output voltage is set by an external resistor divider R3 and R4 in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of R3 can be calculated by equation 5.

$$_1 = \frac{(\quad - \quad) \times \ _2}{} \qquad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.0V

Table 3. Feedback Resistor R_1 R_2Value for Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
5 V		
9 V		
12 V		

Inductor Selection

The performance of
and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boost converter, calculate the inductor DC current as in equation 6

$$= \frac{\times}{\times} \quad (6)$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
-

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in equation 7

$$= \frac{1}{\times \left(\frac{1}{-} + \frac{1}{}\right) \times} \quad (7)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation 8.

$$= \quad + \frac{}{2} \quad (8)$$

Set the current limit of the SCT1271 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed
d ESR resistance, and its footprint.
Shielded inductors typically have higher DCR than unshielded inductors. Table 4 lists recommended inductors for the SCT1271. Verify whether the recommended inductor can support the user's target application with the previous

calculations and bench evaluation. In this application, the Wurth-Elektronix 's inductor 744313220 is used on SCT1271 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max H	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744325180	1.8	3.5	18 / 14	10.5 x 10.2 x 4.7	Wurth Elektronix
744311150	1.5	7.2	14 / 11	7.3 x 7.2 x 4.0	Wurth Elektronix
744311220	2.2	12.5	13 / 9	7.3 x 7.2 x 4.0	Wurth Elektronix
744313220	2.2	5.7	18 / 14	12.9 x 12.8 x 3.3	Wurth Elektronix
CDMC8D28NP-1R8MC	1.8	12.6	9.4 / 9.3	9.5 x 8.7 x 3.0	Sumida

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1 recommended to be placed as close as possible to the VIN pin of the SCT1271. A ceramic capacitor of more than 1.0 internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22 input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, three 22 ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 9 and 10 to calculate the minimum required effective capacitance, C_{OUT}.

$$= \frac{(\quad - \quad _{-} \quad) \times}{\times \quad \times} \tag{9}$$

$$= \quad \times \tag{10}$$

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- $_{SW}$ is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

Loop Stability

An external loop compensation network comprises resister R5, ceramic capacitors C5 and C6 connected to the COMP pin

$$_6 = \frac{\times}{5} \quad (18)$$

If the calculated value of C6 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Waveforms

Vin=3.6V, Vout=9V, unless otherwise noted

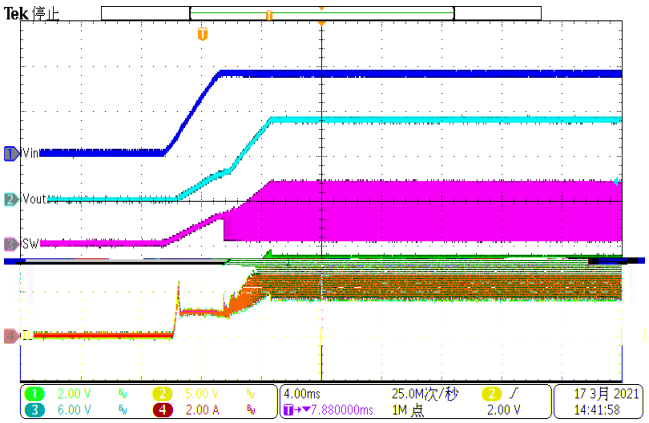


Figure 9. Power up

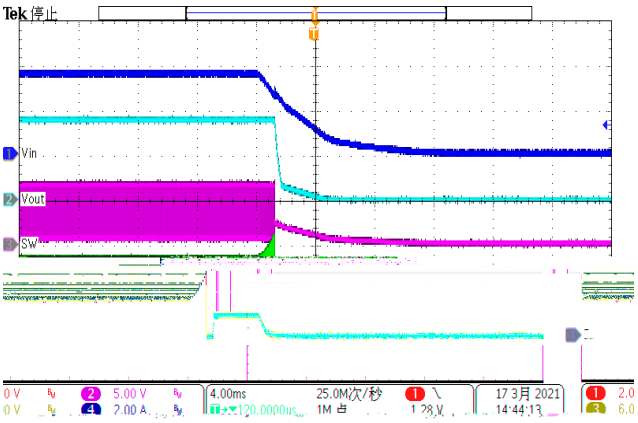


Figure 10. Power down

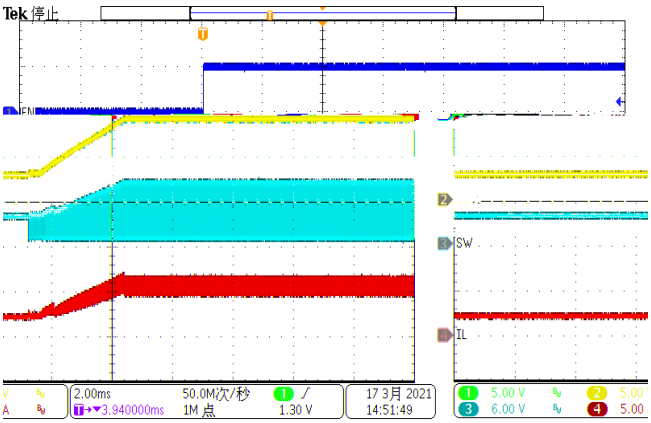


Figure 11. EN Power up (Iload=2A)

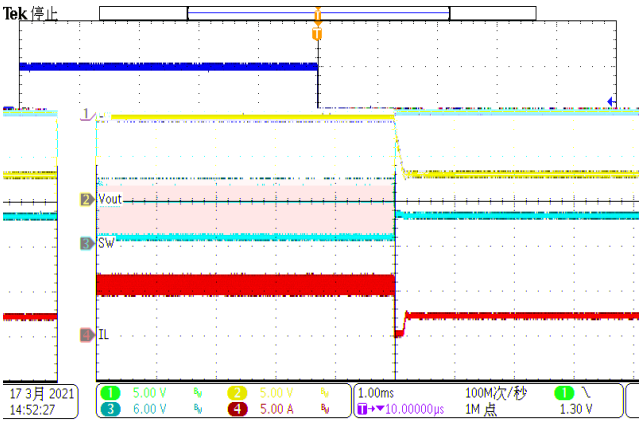


Figure 12. EN Power down(2A)

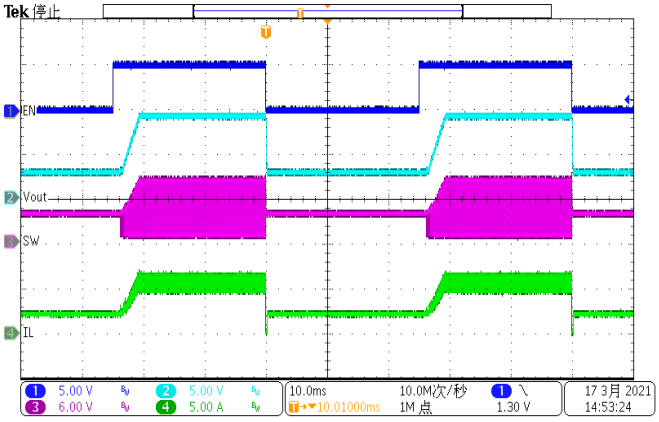


Figure 13. EN toggle (Iload=2A)

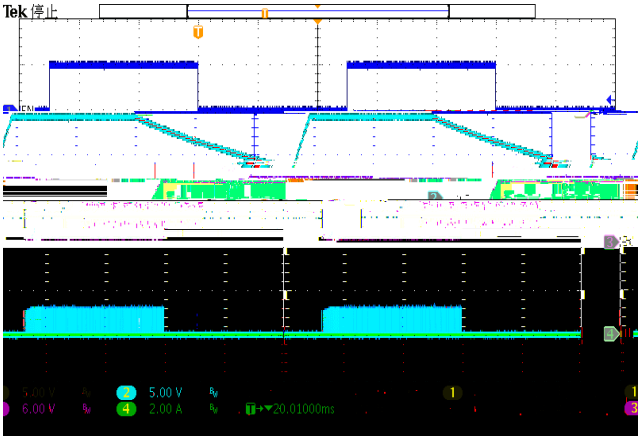


Figure 14. EN toggle (Iload=10mA)

Application Waveforms(continued)

Vin=3.6V, Vout=9V, unless otherwise noted

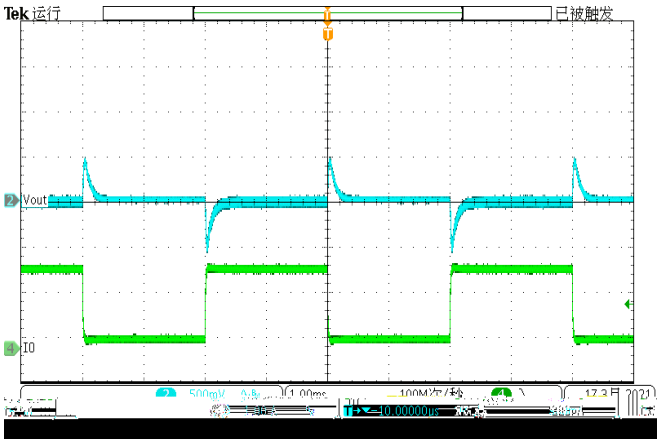


Figure 15. Load transient (0.2A-1.8A, 1.6A/us)

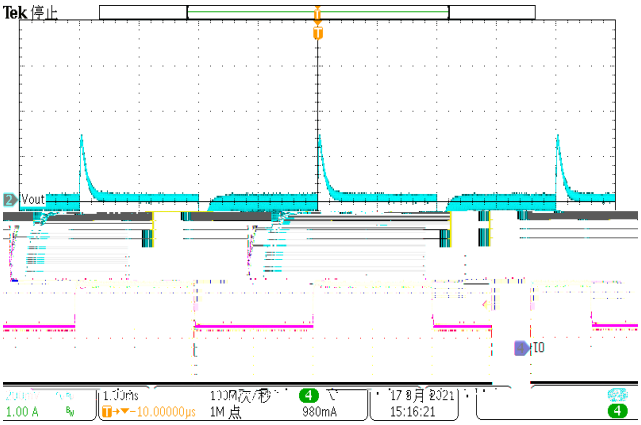


Figure 16. Load transient (0.5A-1.25A, 1.6A/us)

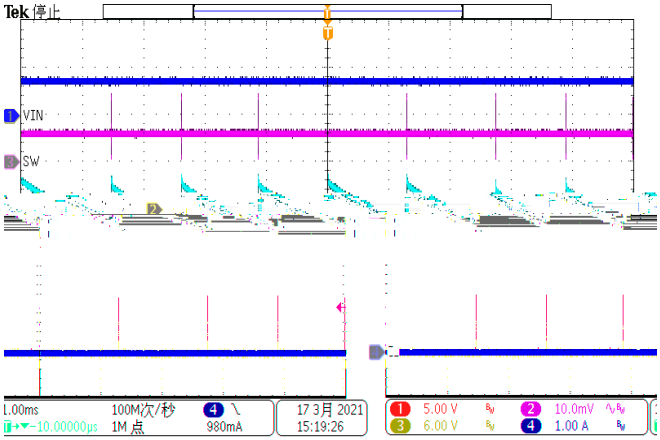


Figure 17. Steady state (Iload=0A, PFM)

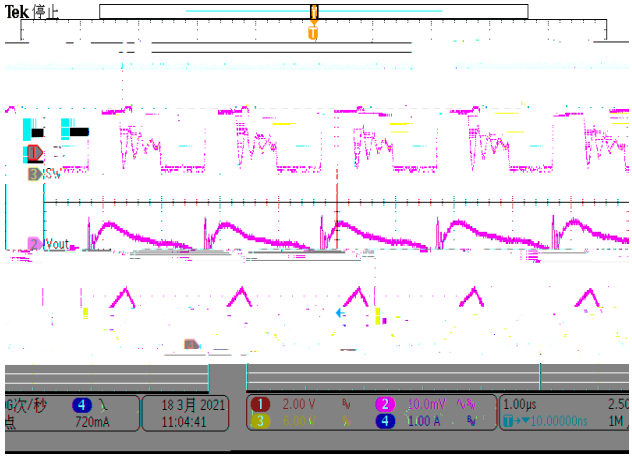


Figure 18. Steady state (Iload=150mA, PFM)

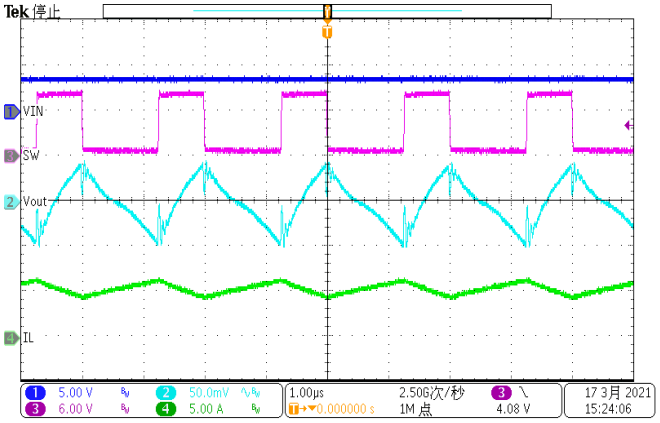


Figure 19. Steady state (Iload=2A)

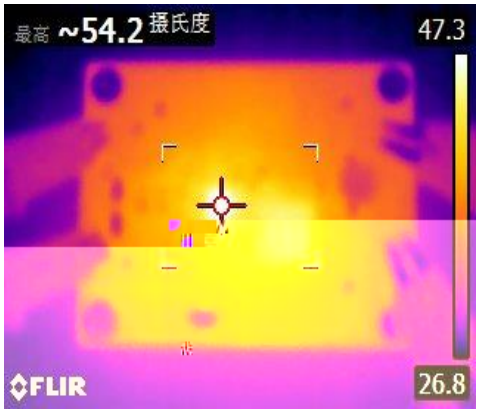


Figure 20. Thermal, Vin=3.6V, Vout=9V, Iload=2A

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin. The placement and ground trace for output capacitor is critical for the performance of SW ringing voltage. Place the 0.1uF output capacitor as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin.

The layout should also be done with well consideration of the thermal. The SW, VOUT and GND pad under the chip should always be soldered well to the board for thermal, mechanical strength and reliability. Improper soldering will cause SW higher ringing and overshoot besides downgrading thermal performance.

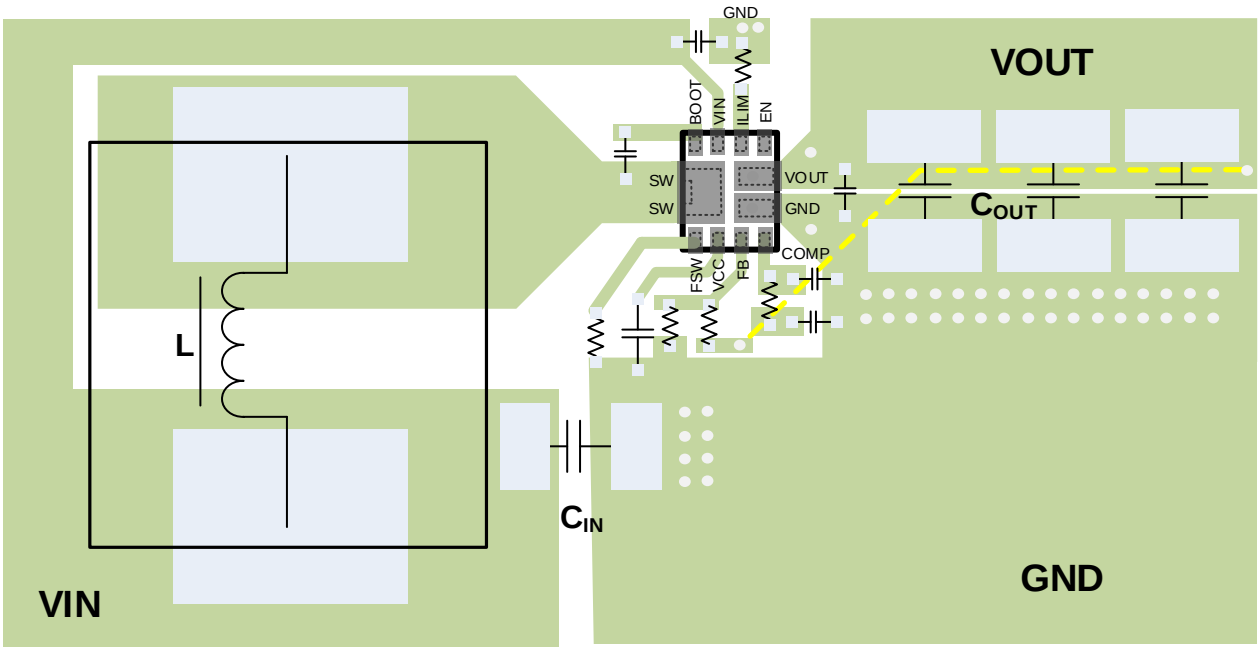


Figure 21. PCB Layout Example Top Layer

Thermal Considerations

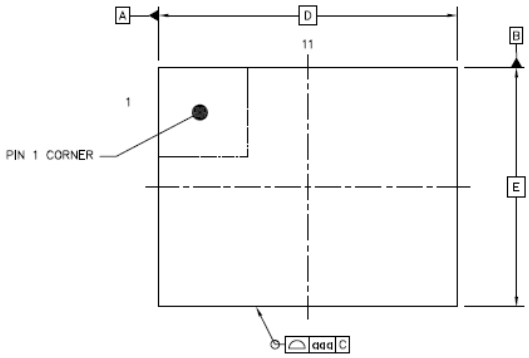
The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 19.

$$(\quad) = \frac{150 -}{\theta JA} \tag{19}$$

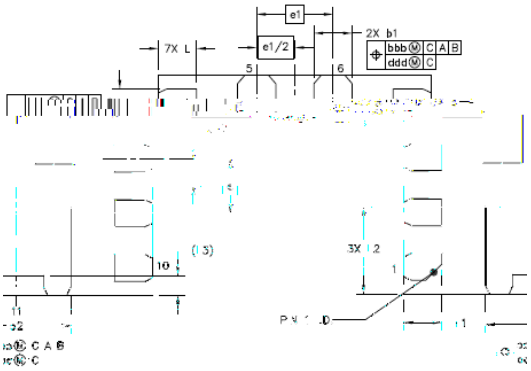
where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

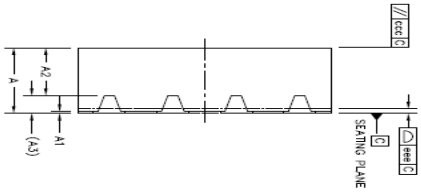
SCT1271 QFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	---	0.55	---
A3		0.203 REF	
b	0.20	0.25	0.30
b1	0.30	0.35	0.40
b2	0.95	1	1.05
D		2.5 BSC	
E		2 BSC	
e		0.5 BSC	
e1		0.7 BSC	
L	0.3	0.35	0.4
L1	0.25	0.35	0.45
L2	0.75	0.8	0.85
L3		0.18 REF	
aaa		0.1	
ccc		0.1	
eee		0.05	
bbb		0.1	
ddd		0.05	

Device	Package Type	Pins	SPQ
SCT1271FQAR	QFN 2.5x2x0.75	11	3000