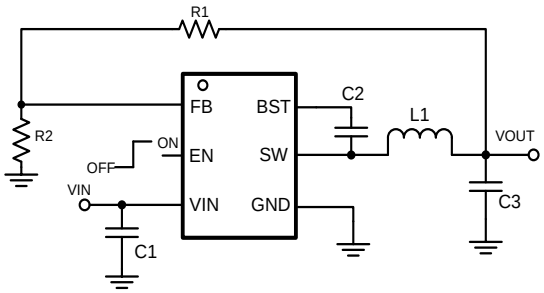
- Switching Node Ringing-free
- 500kHz Switching Frequency
- Pulse Skipping Mode in Light Load Condition
- 3.8V-32V Wide Input Voltage Range
- Up to 2A Continuous Output Load Current
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 130 R_{dson} High Side MOSFET and 70 R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Dropout Mode Operation
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in TSOT23-6L Package

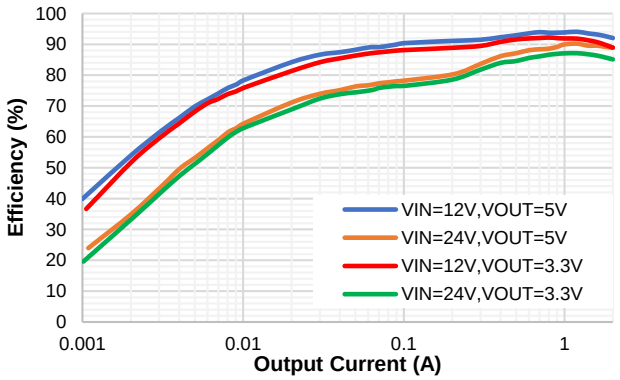
- White Goods, Home Appliance
- Surveillance
- Audio, WiFi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display

The SCT2322 is 2A synchronous buck converters with up to 32V wide input voltage range, which fully integrates a 130 -side MOSFET and a 70 low-side MOSFET to provide high efficiency step-down DCDC conversion. The SCT2322 adopts peak current mode control with the integrated compensation network, which makes SCT2322 easily to be used by minimizing the off-chip component count. The SCT2322 supports the Pulse Skipping Modulation (PSM).

The SCT2322 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

The SCT2322 offers output over-voltage protection, cycle-by-cycle peak current limit, and thermal shutdown protection. The device is available in a low-profile TSOT23-6L package.





NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to market

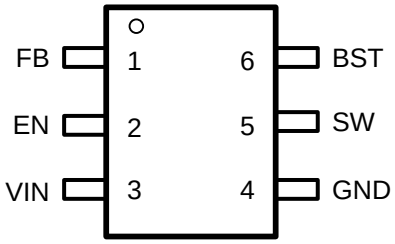
Revision 1.1: Delete VS in ABS table

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2322TVB	2322	TSOT23-6L

1）For Tape & Reel, Add Suffix R (e.g. SCT2322TVBR).

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	40	V
VIN, SW, EN	-0.3	34	V
FB	-0.3	5.5	V
Operating junction temperature(2)	-40	125	°C
Storage temperature T_{STG}	-65	150	°C



Top View: TSOT23-6L, Plastic

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

NAME	NO.	PIN FUNCTION
FB	1	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	2	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.18V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
VIN	3	Power supply input. Must be locally bypassed.
GND	4	Power ground. Must be soldered directly to ground plane.
SW	5	Switching node of the buck converter.

BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.8		32	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		3.5 420	3.7	V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1	3	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		250		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.18	1.25	V
V_{EN_L}	Enable low threshold		1.03	1.1		V
I_{EN}	Enable pin input current	EN=1V	1	1.5	2	uA
I_{EN_HYS}	Enable pin hysteresis current	EN=1.5V		4		uA
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			130		

RN_H

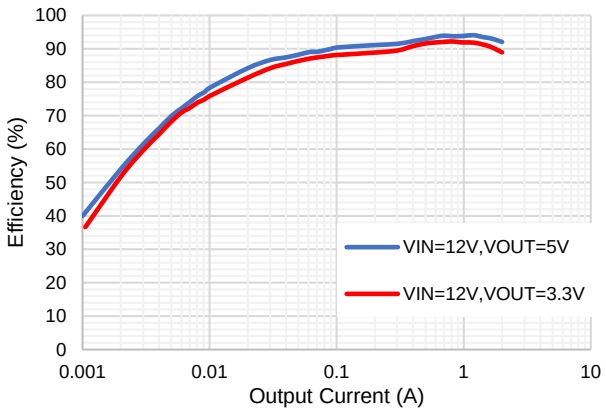


Figure 1. SCT2322 Efficiency, VIN=12V

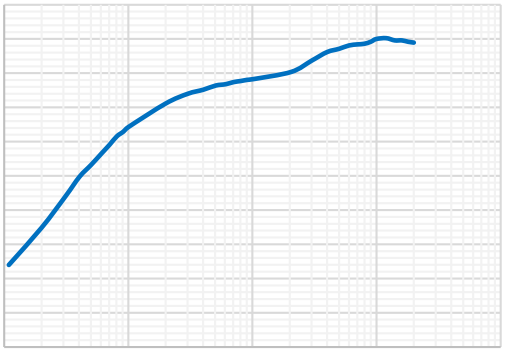


Figure 2. SCT2322 Efficiency, VIN=24V

Figure 3. Shut-down Current vs Temperature

Figure 4. Peak Current Limit vs Temperature

Figure 5. Reference Voltage vs Temperature

Figure 6. VIN UVLO vs Temperature

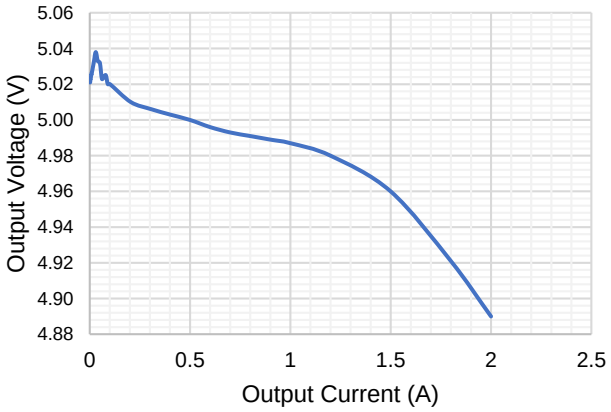


Figure 9. Load Regulation (VIN=24V, VOUT=5V)

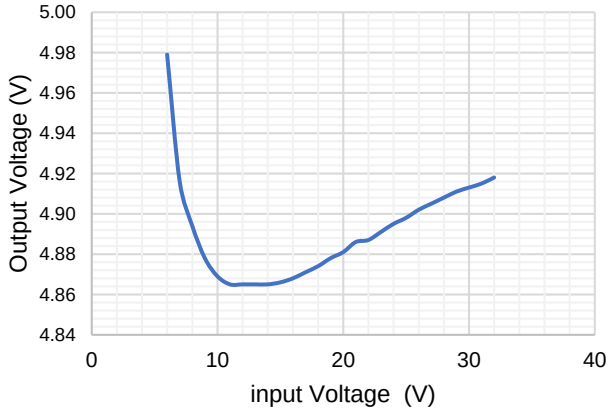
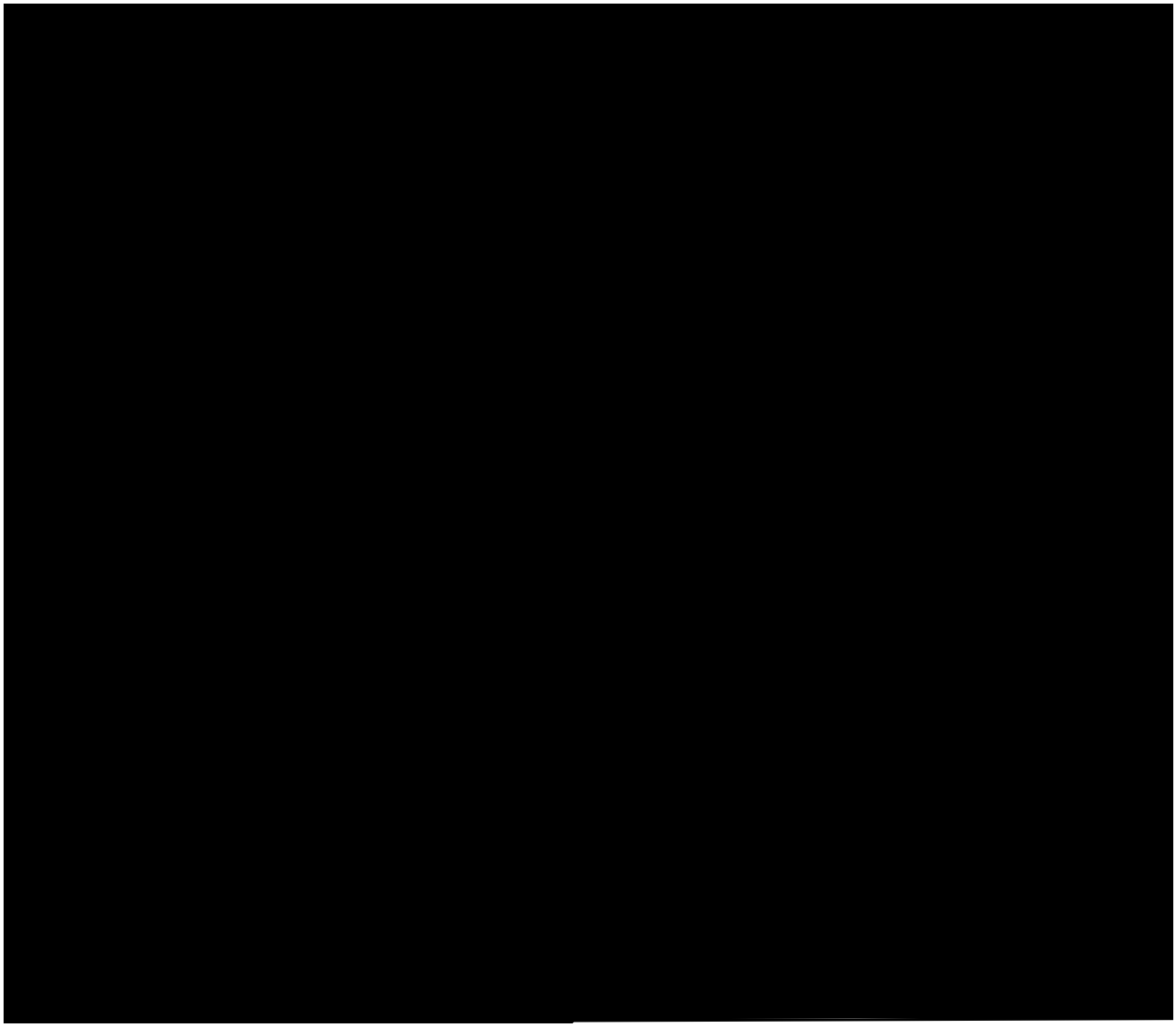


Figure 10. Line Regulation (IOUT=2A)



Overview

The SCT2322 device is 3.8V-32V input, 2A output, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 500kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 4ms soft-start simplify the SCT2322 footprints and minimize the off-chip component counts.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The quiescent current of SCT2322 is 20uA typical under no-load condition and no switching. When disabling the device, the supply shut down current is only 1 The SCT2322 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT2322 device also features full protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

VIN Power

The SCT2322 is designed to operate from an input voltage supply range between 3.8V to 32V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT2322 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable e

Figure 12. SCT2322 Switching Node Waveform

Figure 13. SCT2322 LDO Mode Waveform

Peak Current Limit and Hiccup Mode

The SCT2322 has cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Over Voltage Protection and Minimum On-time

Both SCT2322 features buck converter output over voltage protection (OVP). If the output feedback pin voltage exceeds110% of feedback reference voltage (0.8V), the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 80ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

PSM Working Modes

In heavy load condition, the SCT2322 forces the device operating at forced Pulse Width Modulation (PWM) mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT2322 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-out Regulation

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT2322. The Low Drop Out Operation is triggered automatic when the off time of the high-side power MOSFET exceeds the minimum off time limitation.

In low drop out operation, high-side MOSFET remains ON as long as the BST pin to SW pin voltage is higher than BST UVLO threshold. When the voltage from BST to SW drops below 2.35V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Only 100ns of low side MOSFET turning on in each refresh cycle minimizes the output voltage ripple. Low-side MOSFET may turn on for several times till bootstrap voltage is charged to higher than 2.7V for high-side

MOSFET working normally. Then high-side MOSFET turns on and remains on until bootstrap voltage drops to trigger bootstrap UVLO again. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high even approaching 100% as shown in Figure 13.

During ultra-low voltage difference of input and output voltages, i.e. the input voltage ramping down to power down, the output can track input closely thanks to LDO operation mode.

Thermal Shutdown

Once the junction temperature in the SCT2322 exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 135°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

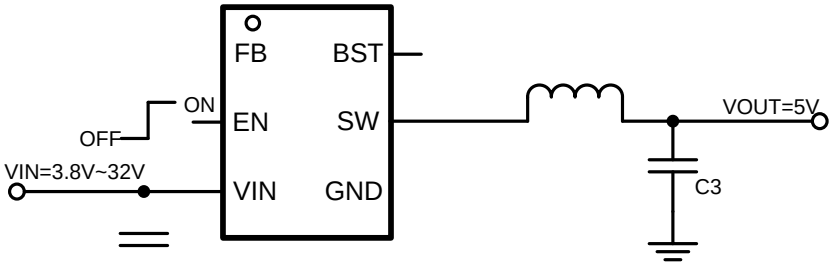


Figure 14. 24V Input, 5V/2A Output

Design Parameters

Design Parameters	Example Value

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10
for the decoupling capacitor anda0.1 to be placed as close as possible to the VIN pin of the SCT2322.

Use Equation (3) to calculate the input voltage ripple:

(3)

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of avior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

(4)

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation (5).

(5)

Set the current limit of the SCT2322 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT2322. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744314101 is used on SCT2322 evaluation board.

Table 1. Recommended Inductors

Part Number	L (uH)	DCR Max (mΩ)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744314101	10	33	3.5	7x7x5	Wurth Electronik

Output Capacitor Selection

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1 3x 22
can be used to improve the load transient response. Due to a capacitor de-rating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

From the required output voltage ripple, use the equation (6) to calculate the minimum required effective capacitance, C_{OUT}.

(6)

Where

- $V_{OUTRipple}$ is output voltage ripple caused by charging and discharging of the output capacitor.
- I_{LPP} is the inductor peak to peak ripple current, equal to $k_{IND} * I_{OUT}$.
- $_{SW}$ is the converter switching frequency.

The allowed maximum ESR of the output capacitor is calculated by the equation (7).

(7)

The output capacitor affects $_{C}$. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency less than 55 kHz (—) without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation (8), assuming C_{OUT} has small ESR.

(8)

Where

- G_M is the transfer conductance of the error amplifier (300uS).

- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

(9)

Output Feed-Forward Capacitor Selection

The SCT2322 has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c. Equation (10) is used to calculate the feed-forward capacitor.

(10)

Output Feedback Resistor Divider Selection

The SCT2322 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure17. Use equation (11) to calculate the resistor divider values.

(11)

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.

Application Waveforms

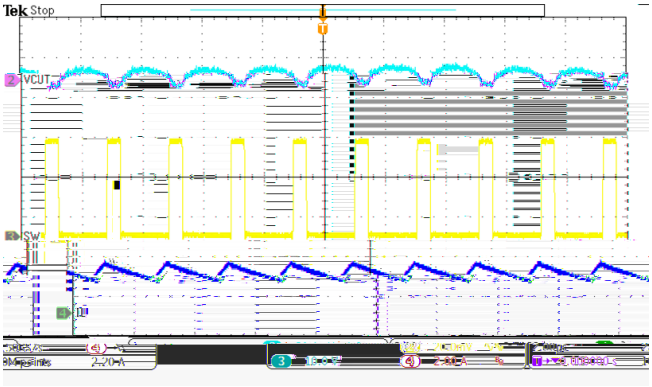


Figure 15. SW node waveform and Output Ripple
VIN=24V, IOUT=2A

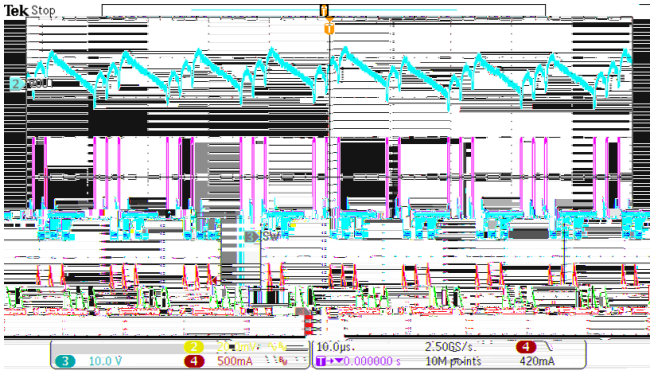


Figure 16. SW node Waveform and Output Ripple
VIN=24V, IOUT=100mA

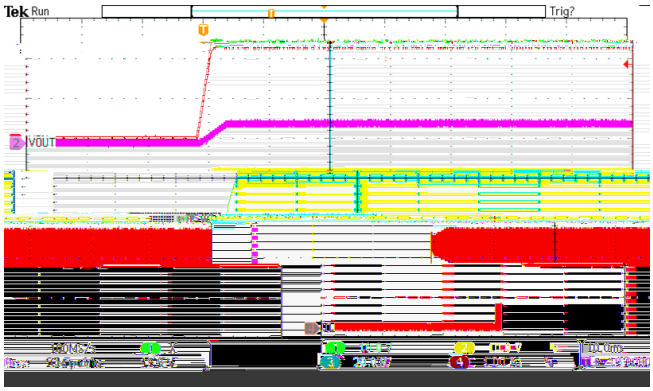


Figure 17. Power Up
VIN=24V, VOUT=5V, IOUT=2A

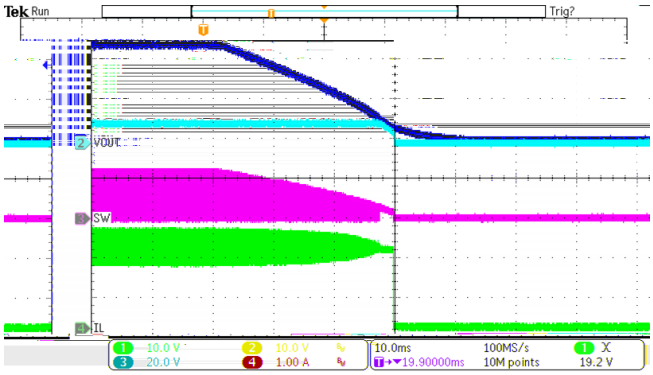


Figure 18. Power Down
VIN=24V, VOUT=5V, IOUT=2A

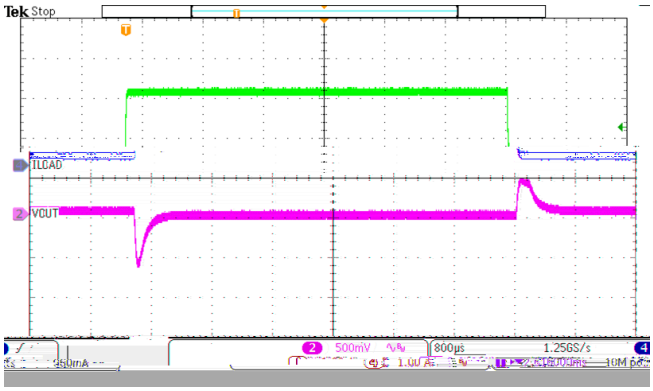


Figure 19. Load Transient
VOUT=5V, IOUT=0.2A to 1.8A, SR=250mA/us

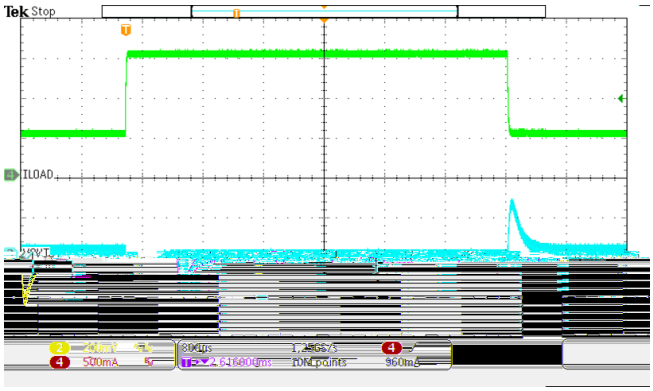


Figure 20. Load Transient
VOUT=5V, IOUT=0.5A to 1.5A, SR=250mA/us

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 21 is the recommended PCB layout of SCT2322.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

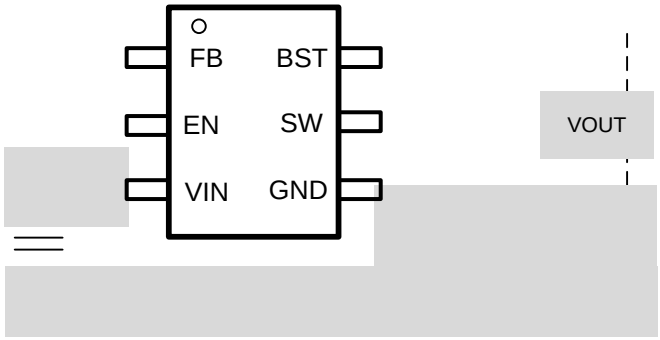


Figure 21. PCB Layout Example

Thermal Considerations

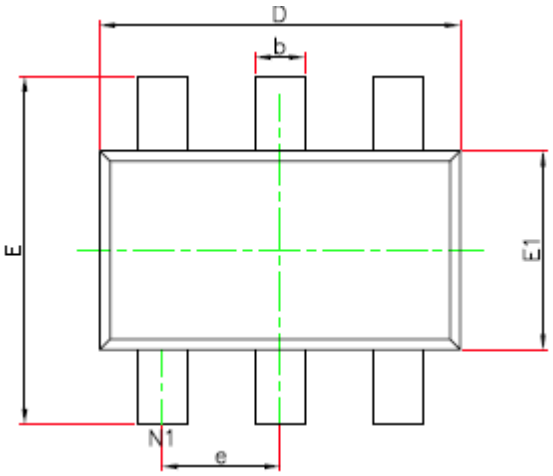
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (12).

(12)

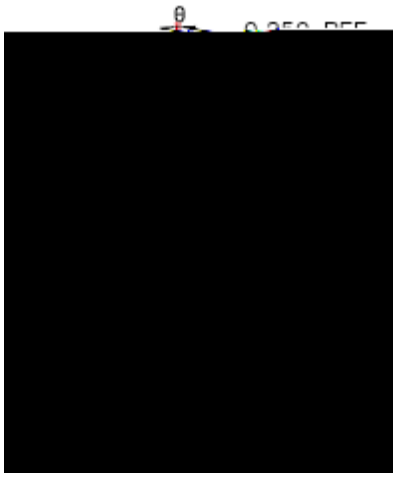
where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

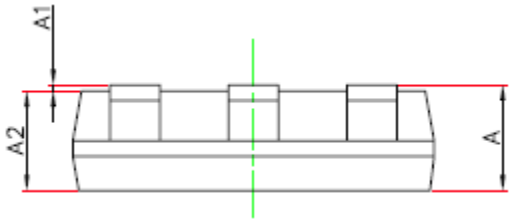
The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.



TOP VIEW



BOTTOM VIEW

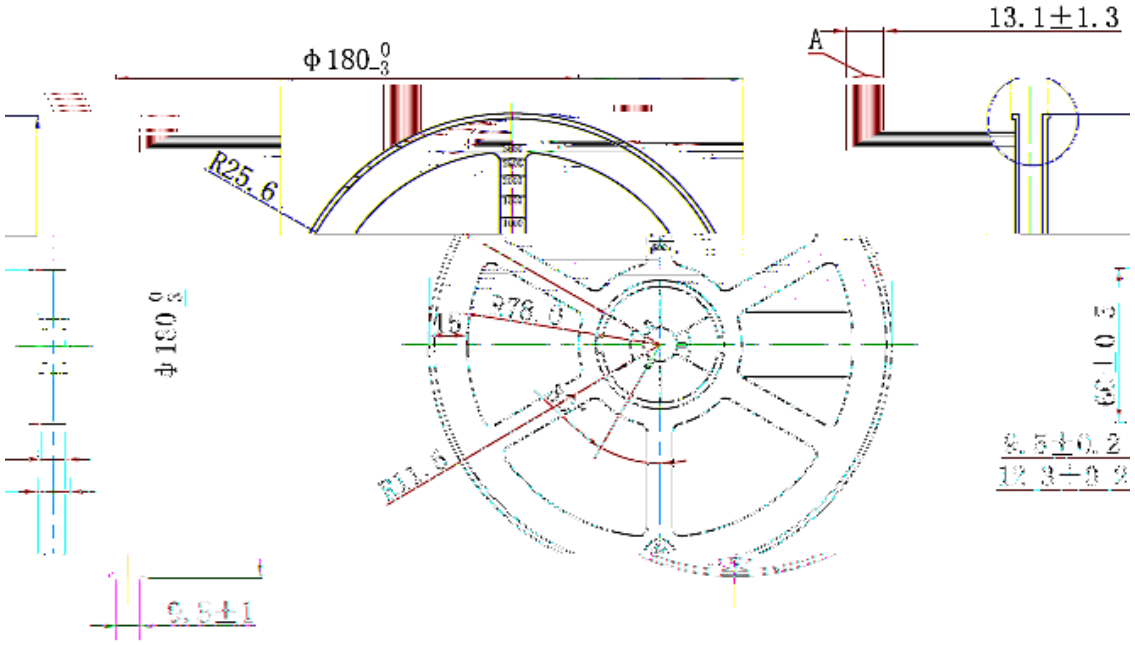


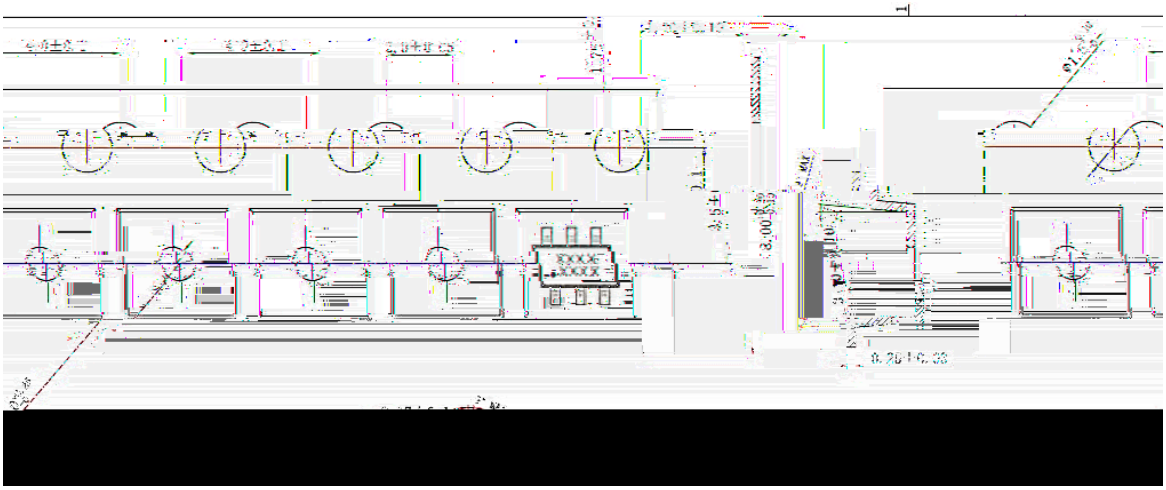
SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	-------		1.10

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.





Feeding Direction

PN	DESCRIPTION	COMMENTS
SCT2325 **SCT2323**	3.8V-32V Vin, Fixed Vout, 2A Synchronous Buck Converter with EMI Reduction	• 1.1MHz switching frequency with ±6% FSS • EMI reduction with switching node ringing-free. • SW anti-ringing in discontinuous current mode • 20uA ultra-low quiescent current • Minimum external components. Easy-to-use • Fixed 5V Vout (SCT2325) and 3.3V Vout (SCT2323)
SCT2330 **SCT2331**	3.8V-32V Vin, 3A Synchronous Step-down DCDC Converter with EMI Reduction	• 500KHz switching frequency • 3A Continuous output current • EMI reduction with switching node ringing-free. • Ultra-low quiescent current. High efficiency PFM at light load (SCT2330) • Frequency Spread Spectrum (SCT2330) • Fixed PWM mode for lower output ripple (SCT2331)

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